

Rocket BSW 11.6" Schematic

Braswell

2015-11-09
REV : A00

DY : None Installed
OSP/ISP : different config for storage and DRAM
Drax : stuff on Drax

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Rocket BSW 11.6"

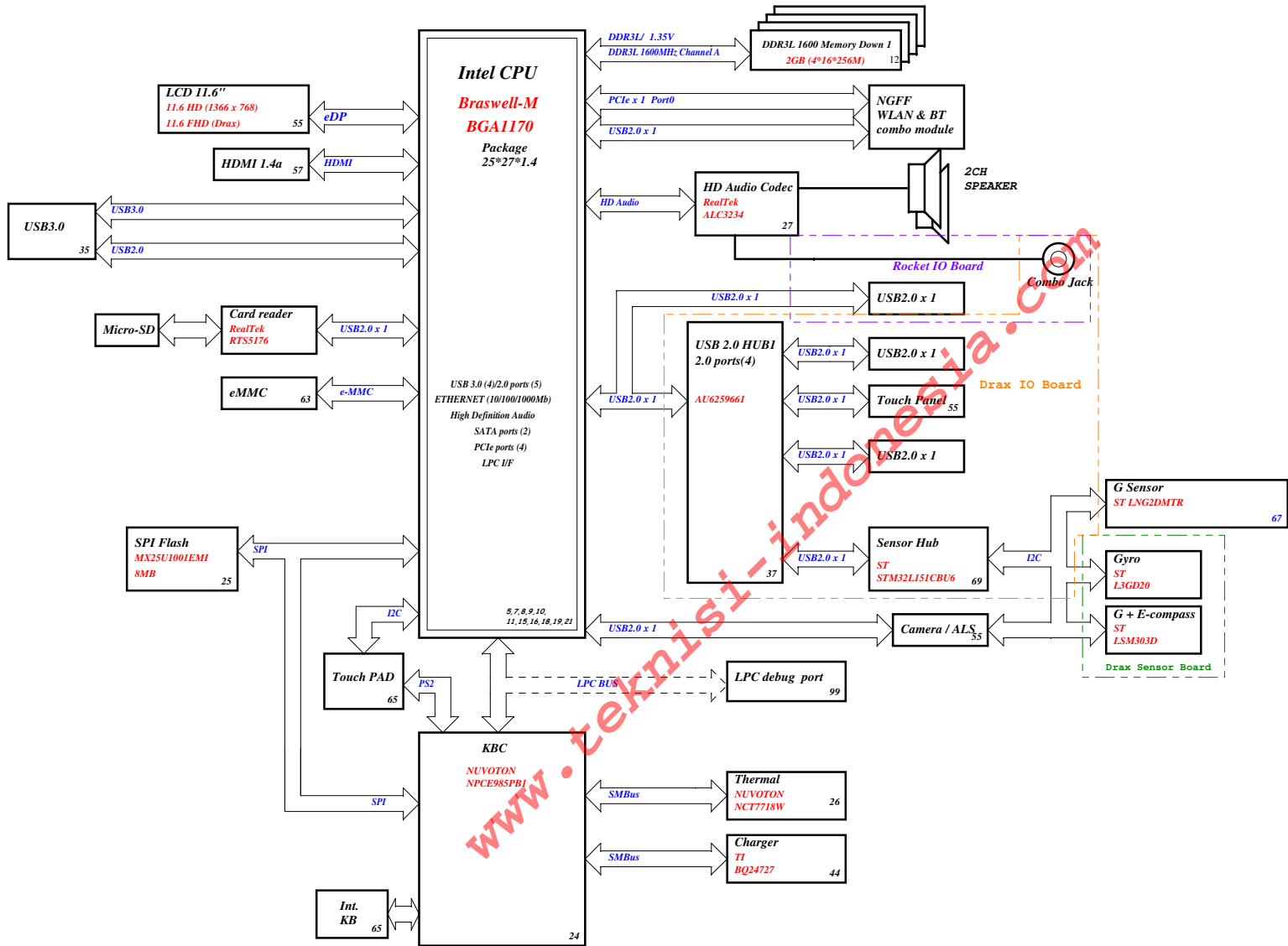
Rev
A00

Date: Monday, November 09, 2015

Sheet 1 of 109

Project code : 4PD076010001
PCB P/N : 15235
Revision : -1

Rocket 11.6" Block Diagram - 0SP



CHARGER	
BQ24727R6RR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+
SYSTEM DC/DC	
SY8288CRAC	45
SY8286BRAC	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5
	5V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	6FX_CORE
SYSTEM DC/DC	
SY8286RAC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5
Step Down Regulator	
SYW232DFC	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
SYSTEM DC/DC	
SY8286RAC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM DC/DC	
APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0
Step Down Regulator	
SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5


PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

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SSID = CPU

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SSID = CPU

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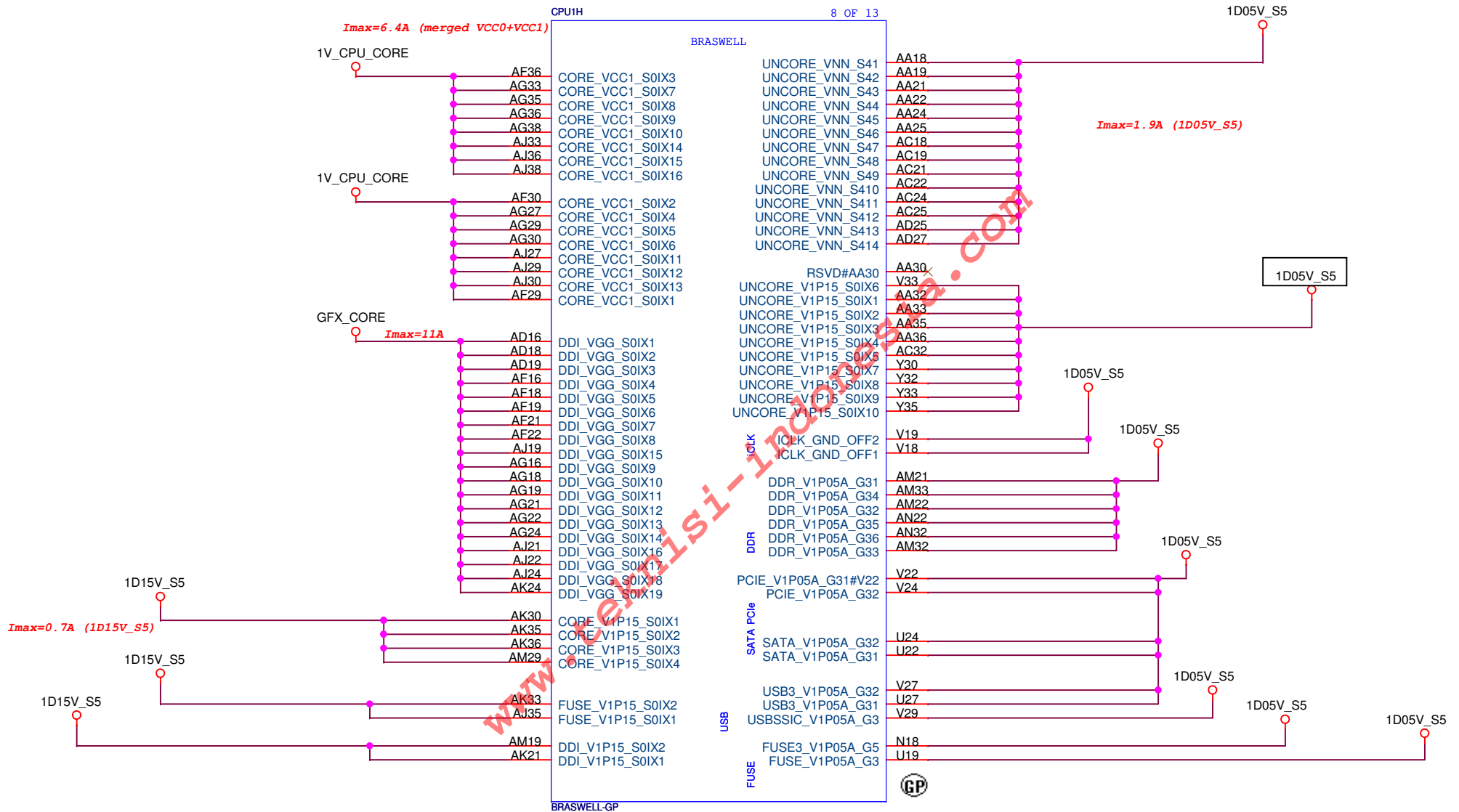
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SSID = CPU



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Title

CPU (VCC CORE)

Size
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Document Number

Rev

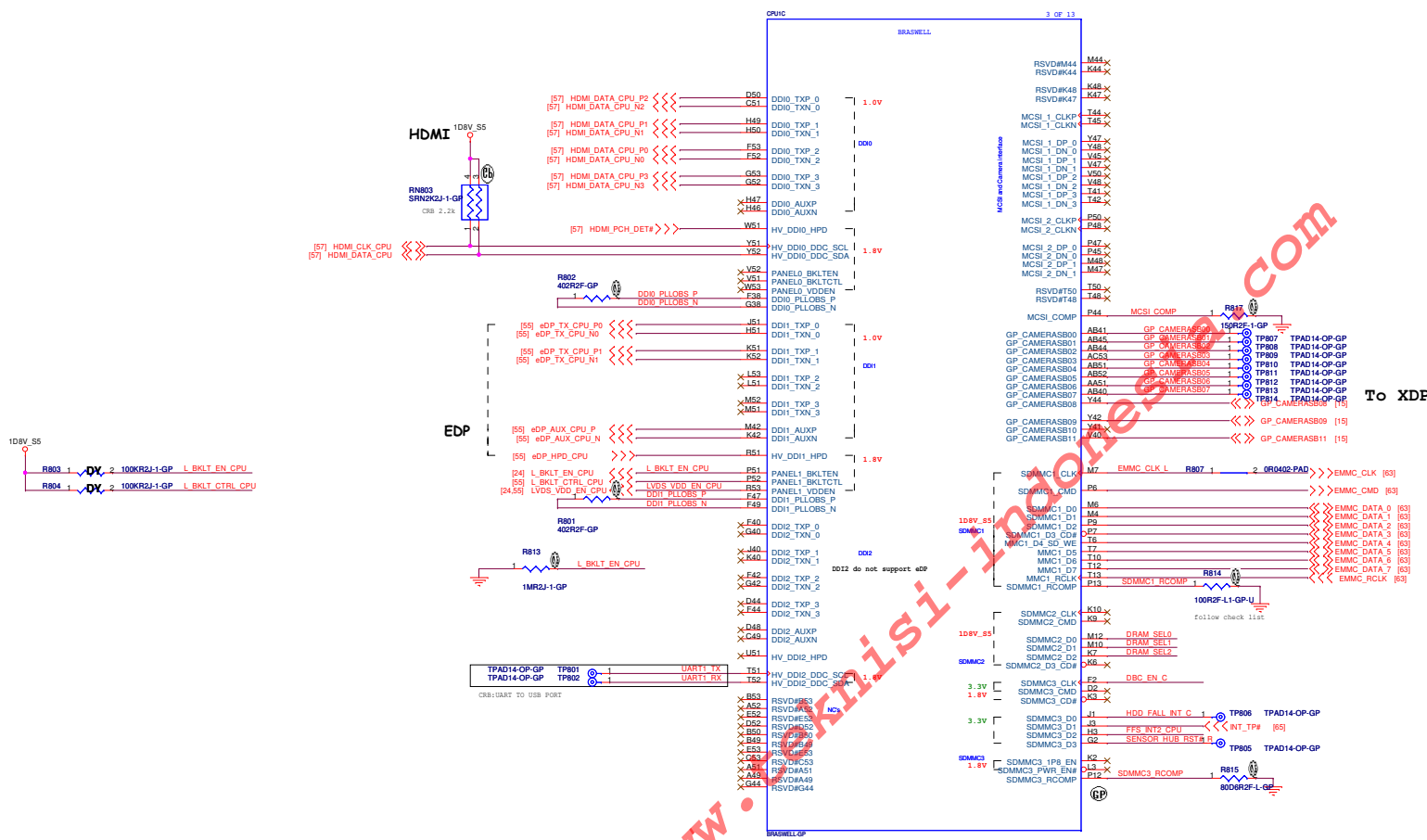
Rocket BSW 11.6"

A00

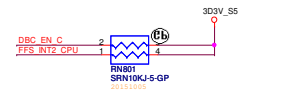
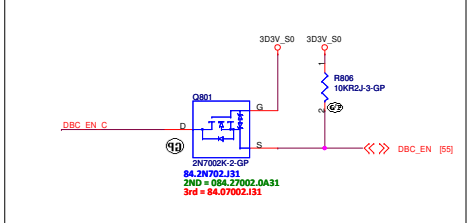
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SSID = CPU

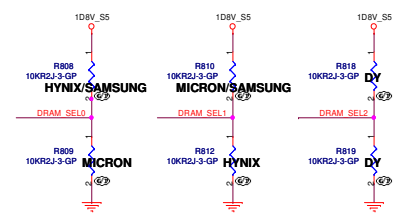


Level Shift

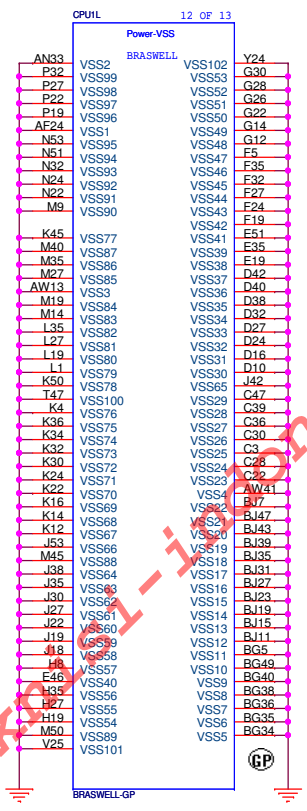
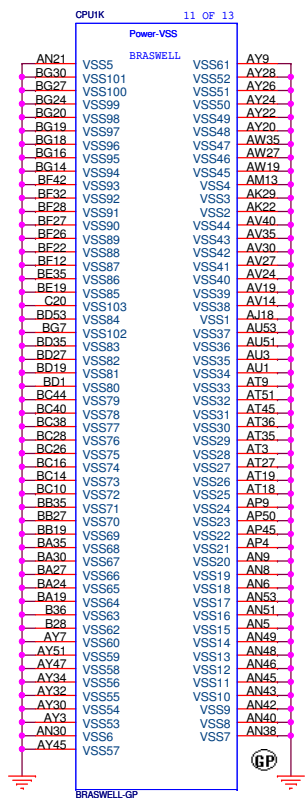
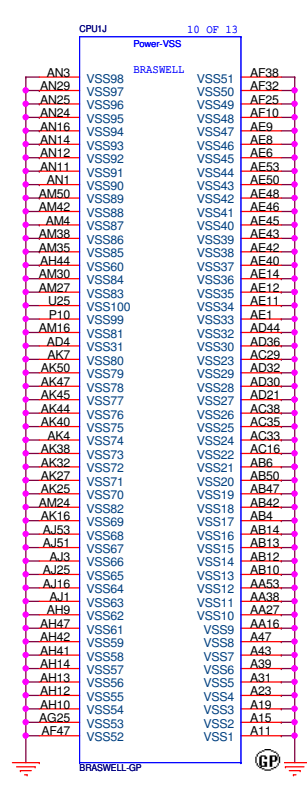


RAM ID bit order is DRAM_SEL2(Reserved), DRAM_SEL1,DRAM_SELO

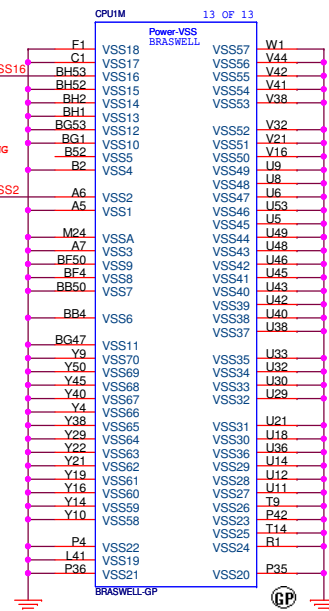
Vender	RAM_ID	Wistron PN	Mfr. PN	Capacity	Freq
So-DIMM	X00				
Hynix	X01	NX80R\$AB	H5TC4G63CFR-PBA	2G	1600MHz
Micron	X10	NX80R\$CA	MT41K256M16HA-125:E	2G	1600MHz
Samsung	X11	NX80R\$BC	K4B4G1646E-BYK0	2G	1600MHz



SSID = CPU



2014/04/25
Intel suggest
TP901 1
TPAD14-OP-GP
CPU VSS16
B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING
TP902 1
TPAD14-OP-GP
CPU VSS2
2014/04/25
Intel suggest



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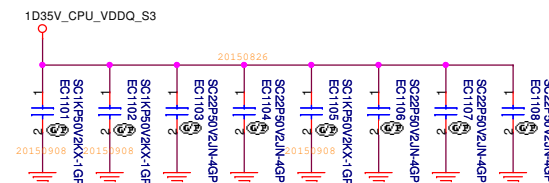
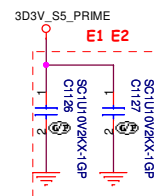
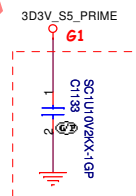
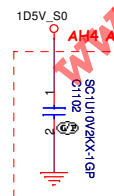
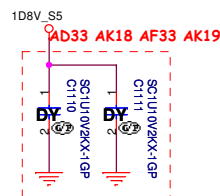
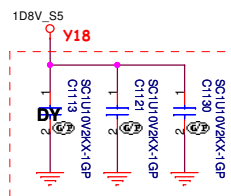
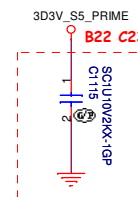
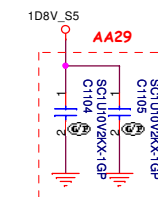
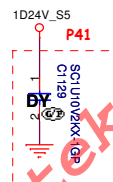
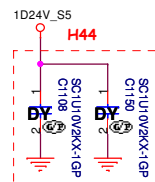
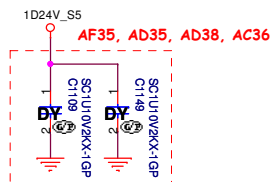
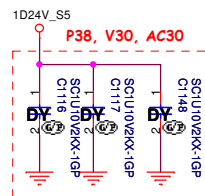
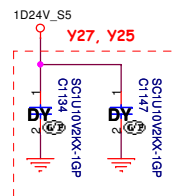
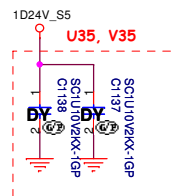
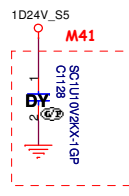
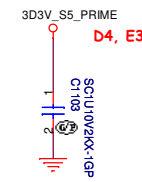
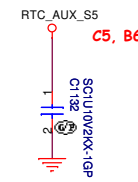
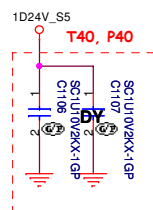
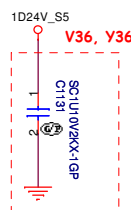
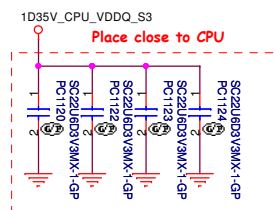
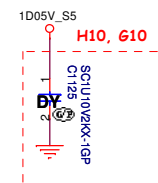
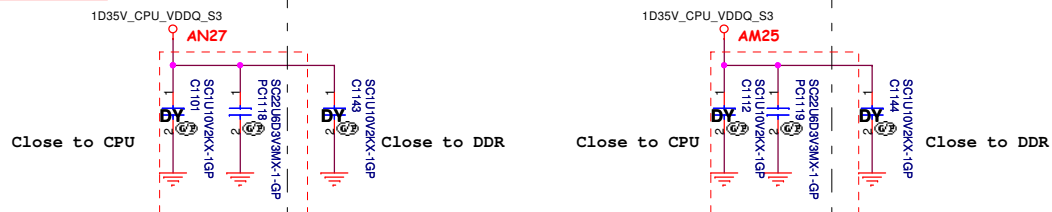
Title
CPU (VSS)

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Rev
A00

SSID = CPU



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CPU (Power CAP2)Size
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SSID = MEMORY

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the
PMC_RSMRST_N signal (check list)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

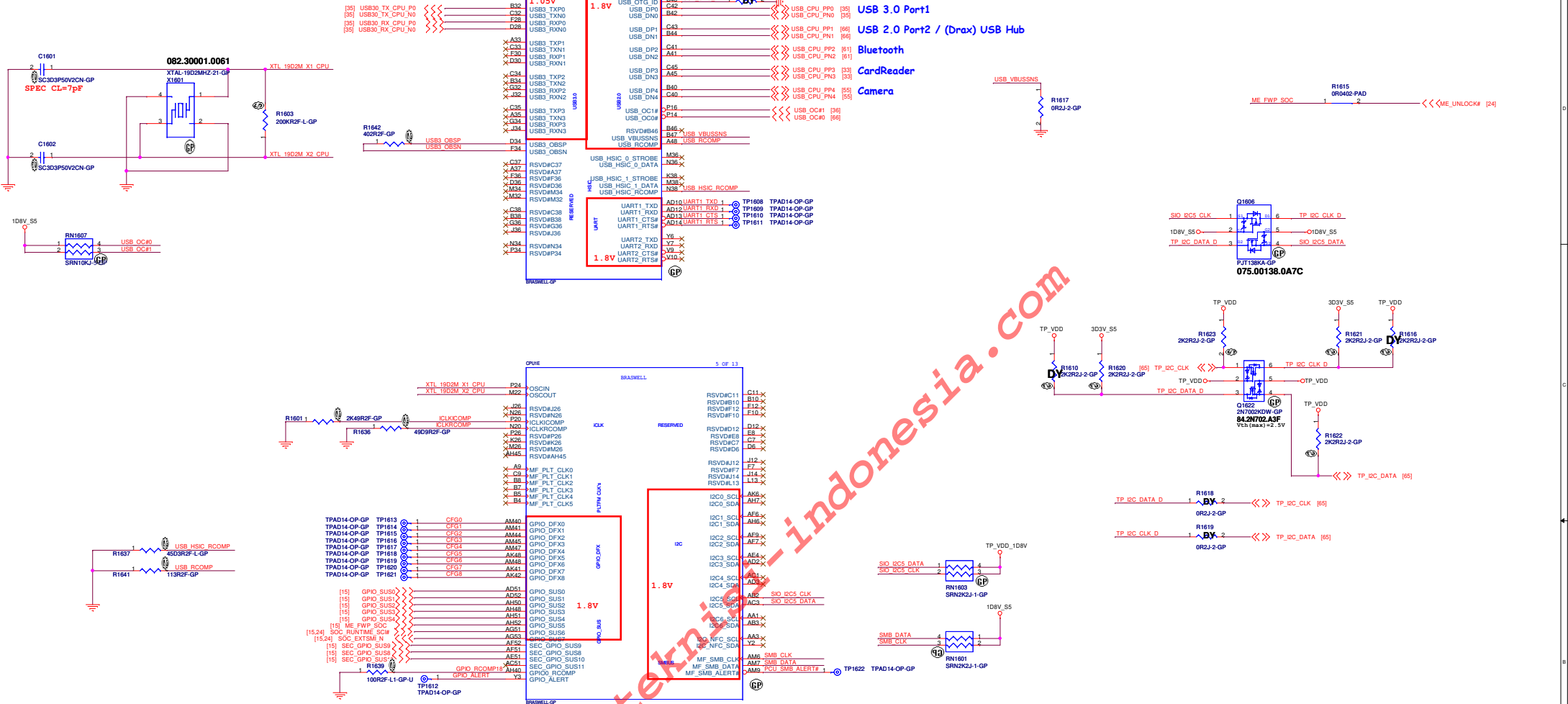
Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (Internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1- Bypass, 0- No bypass	Low

SSID = PCH

Level shift



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Size A2	Document Number	Rev	A00
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SSID = CPU

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Size
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Date: Monday, November 09, 2015

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A00

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SSID = PCH

WLAN

[61] PCIE_TX_CON_P0
[61] PCIE_TX_CON_N0
[61] PCIE_RX_CPU_P0
[61] PCIE_RX_CPU_N0

C1915 2
C1916 2

1 SCD1U16V2KX-3GP
1 SCD1U16V2KX-3GP

PCIE_TX_CPU_P0
PCIE_TX_CPU_N0

C24
B24
G20
J20

PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0

1.0V

PCIE

A25
C25
D20
F20

PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1

B26
C26
D22
F22

PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2

A27
C27
G24
J24

PCIE_TXP3
PCIE_TXN3
PCIE_RXP3
PCIE_RXN3

PCIE_CLKREQ0_CPU#
PCIE_CLKREQ1_CPU#
PCIE_CLKREQ2_CPU#
PCIE_CLKREQ3_CPU#

AM10
AM12
AK14
AM14

1.8V

PCIE_CLKREQ0#
PCIE_CLKREQ1#
PCIE_CLKREQ2#
PCIE_CLKREQ3#

A21
C21
B20
C18
B18
C17
A17
C16
B16

CLK_DIFF_P_0
CLK_DIFF_N_0
CLK_DIFF_P_1
CLK_DIFF_N_1
CLK_DIFF_P_2
CLK_DIFF_N_2
CLK_DIFF_P_3
CLK_DIFF_N_3
CLK_DIFF_P_4
CLK_DIFF_N_4

PCIE_OBSP CPU
PCIE_OBSN CPU

D26
F26

PCIE_OBSP
PCIE_OBSN

1.8V

SPI

V14
Y13
Y12
Y13
Y12

SPI1_CLK
SPI1_CS0#
SPI1_CS1#
SPI1_MISO
SPI1_MOSI

1.8V

BRASWELL-GP

GP

GP

GP

GP

GP

GP

GP

4 OF 13

BRASWELL

GP

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GP

GP

GP

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GP

GP

GP

GP

1.8V

SATA

SATA_LED#
SATA_GP0
SATA_GP1
SATA_GP2
SATA_GP3

AH3
AH2
AG3
AG1
AF3

SATA_OBSP
SATA_OBSN

N30
M30

1.8V

FST_SPI_CLK#

W3
V4
V6
V7

SPI_CLK_CPU
SPI_CS_CPU_N0
SPI_SI_CPU
SPI_SO_CPU

R1911 1
R1909 1
R1910 1

10R2J-2-GP
33R2J-2-GP
10R2J-2-GP

SPI_CLK_ROM [25]
SPI_CS_ROM_N0 [25]
SPI_SI_ROM [25]
SPI_SO_CPU [25]

SPI_WP_CPU [25]
SPI_HOLD_CPU [25]

1.5V

MF_HDA_RST#
MF_HDA_SD1#
MF_HDA_CLK#
MF_HDA_SD10
MF_HDA_SYNC
MF_HDA_SDO
MF_HDA_DOCKEN#
MF_HDA_DOCKRST#

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SDIN0_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AF13
AD6
AD9
AD7
AF12
AF14
AB9
AB7

1.8V

AUDIO

GP_SSP_2_CLK#
GP_SSP_2_FS
GP_SSP_2_TXD
GP_SSP_2_RXD

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

AK9
AK10
AK12
AK13

HDA_RST# CPU
HDA_BITCLK_CPU
HDA_SYNC_CPU
HDA_SDOUT_CPU

75R2F-2-GP

R1928 1

HDA_RST#_CODEC [27,29]

75R2F-2-GP

R1927 1

HDA_BITCLK_CODEC [27]

75R2F-2-GP

R1926 1

HDA_SYNC_CODEC [27]

75R2F-2-GP

R1925 1

HDA_SDOUT_CODEC [27]

75R2F-2-GP

R1924 1

HDA_RST#_CODEC [27,29]

75R2F-2-GP

R1923 1

HDA_BITCLK_CODEC [27]

75R2F-2-GP

R1922 1

HDA_SYNC_CODEC [27]

75R2F-2-GP

R1921 1

HDA_SDOUT_CODEC [27]

75R2F-2-GP

R1920 1

HDA_RST#_CODEC [27,29]

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

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2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

2N7002K-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

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0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP

0R2J-2-GP


SSID = PCH

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Title

(Reserved)

Size
A4

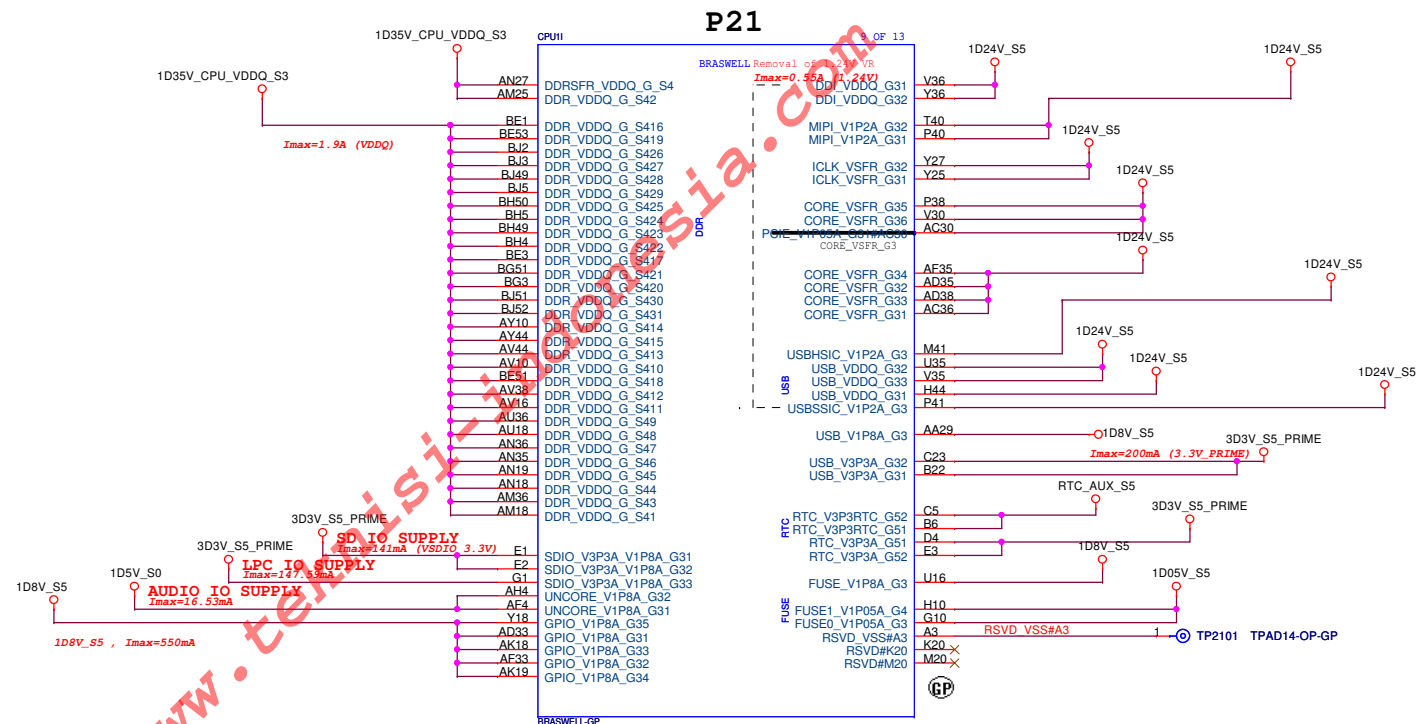
Document Number
Rocket BSW 11.6"

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Rev
A00

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SSID = CPU



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CPU (POWER1)Size
A3

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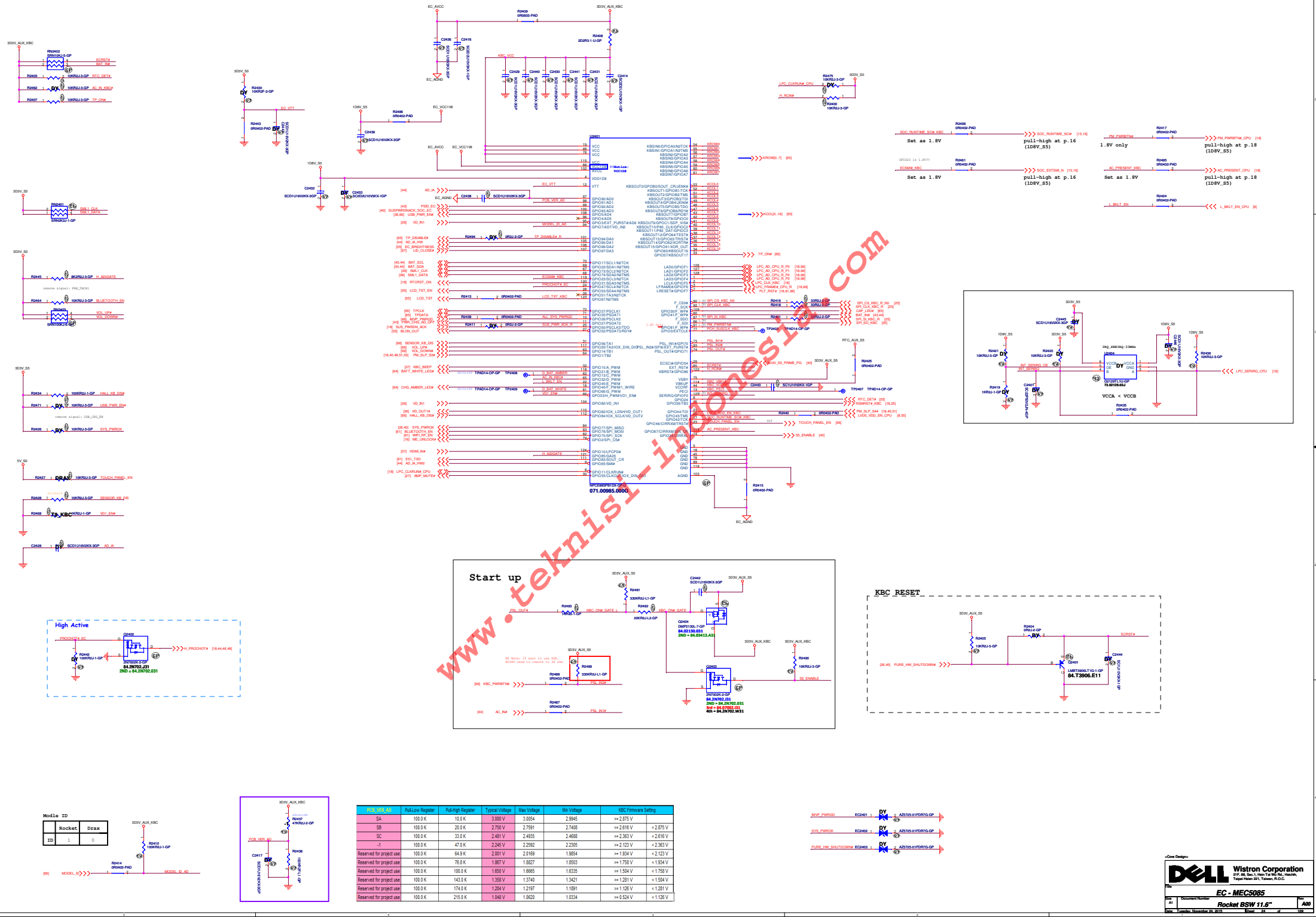
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SSID = KBC

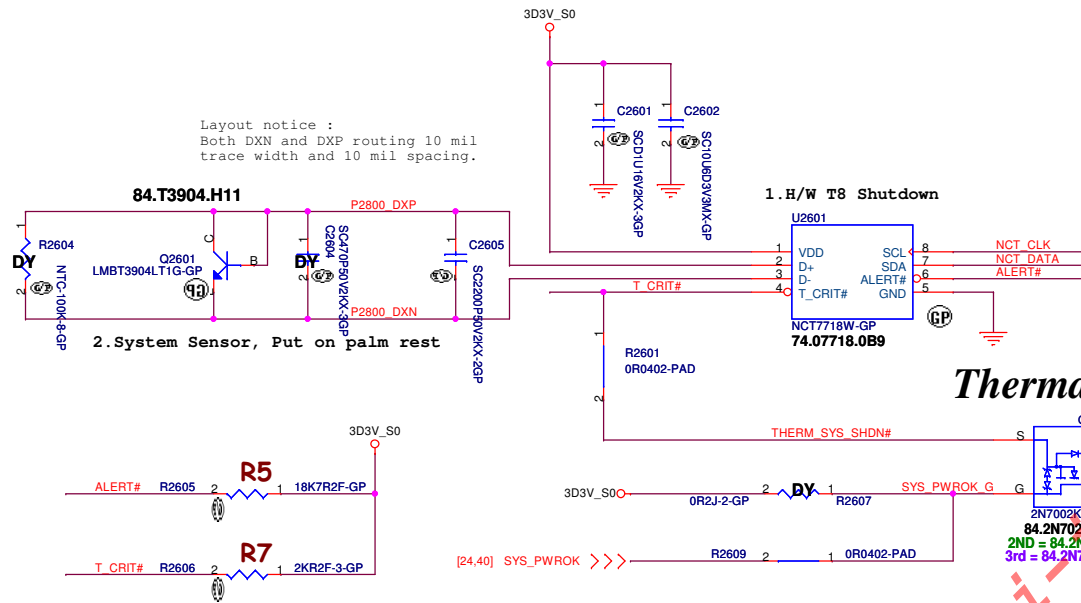


Pin	With ID	Pull/Up Register	Pull/Up Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.975 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7400	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4595	2.4680	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2502	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.894 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.887 V	1.8827	1.8903	>= 1.758 V	< 1.824 V
Reserved for project use	100.0 K	100.0 K	1.850 V	1.8695	1.8335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.350 V	1.3740	1.3421	>= 1.201 V	< 1.594 V
Reserved for project use	100.0 K	174.0 K	1.180 V	1.204 V	1.2197	>= 1.026 V	< 1.381 V
Reserved for project use	100.0 K	215.0 K	1.040 V	1.0620	1.0334	>= 0.924 V	< 1.126 V

SSID = Thermal

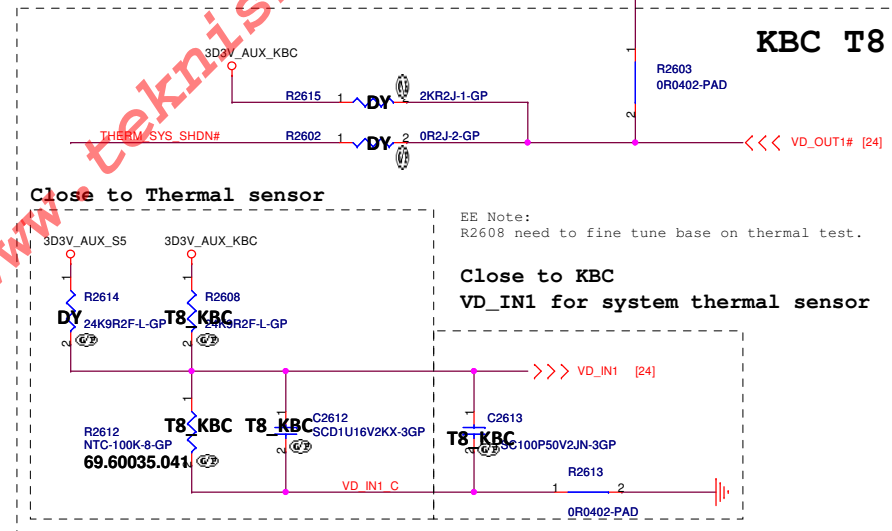
1. T8: PURE_HW_SHUTDOWN# through Q2603.
2. THM_SENSOR: Thermal sensor NCT7718W solution.

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Layout Note: Close U2601



pull-high at p.24
(3D3V_S5)

—<> SML1_DATA [24]

Thermal sensor NCT 7718W

KBC T8

EE Note:
R2608 need to fine tune base on thermal test.

Close to KBC
VD_IN1 for system thermal sensor

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Title

Thermal

Size
A3

Document Number

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Rev
A00


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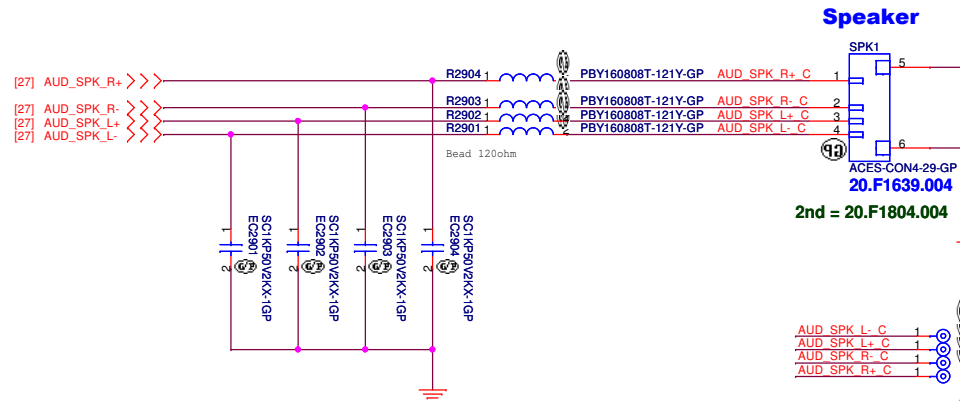
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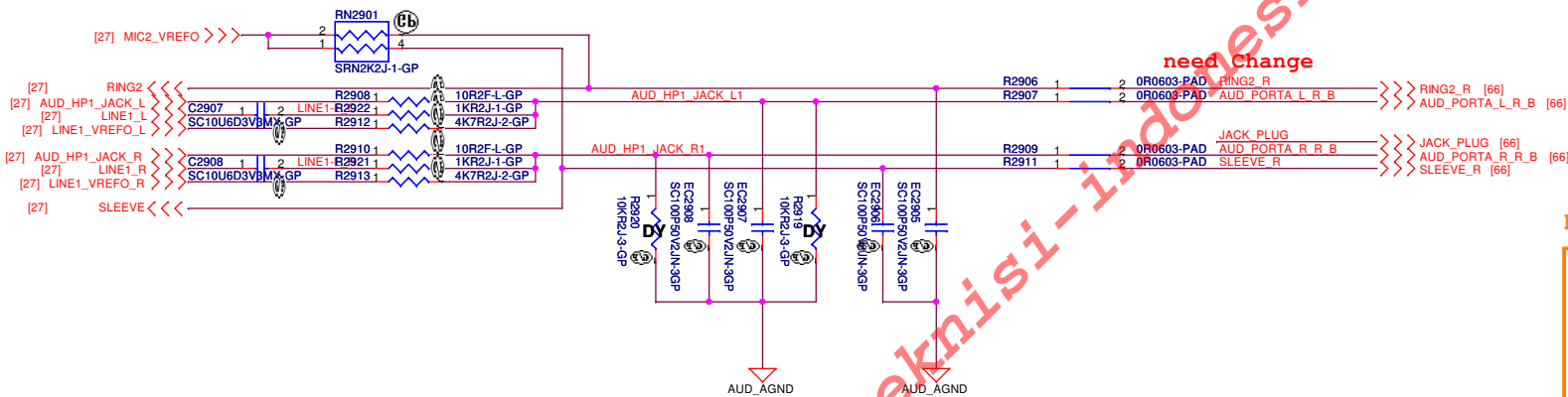
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Title (Reserved)			
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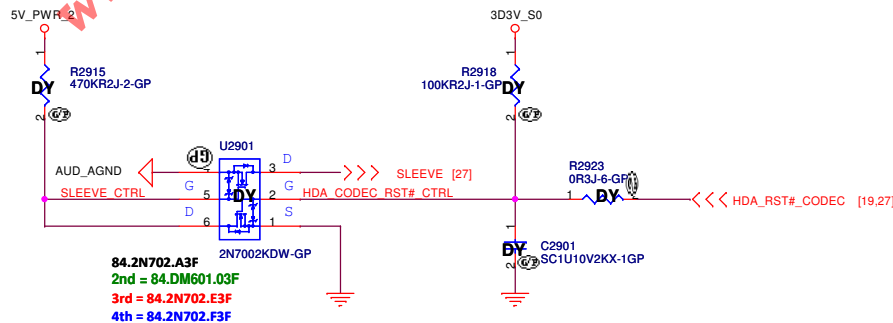
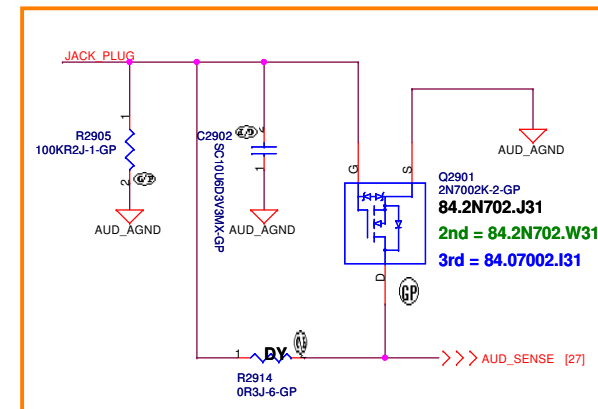
SSID = AUDIO



Combo Jack



Delay circuit



SSID = LOM

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SSID = LAN

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Title (Reserved)LAN			
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SSID = LAN CONN

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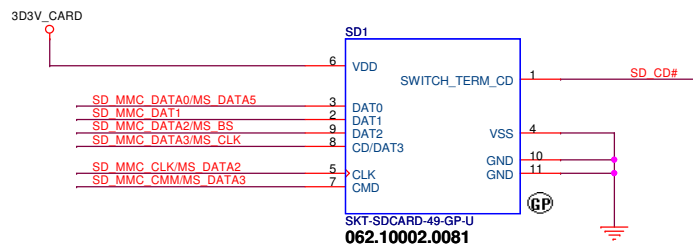
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Title **(Reserved)RJ45+Transformer**

Size A4	Document Number Rocket BSW 11.6"	Rev A00
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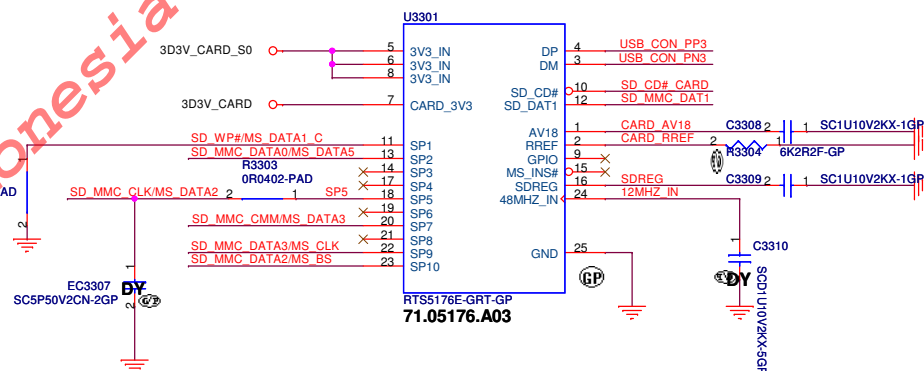
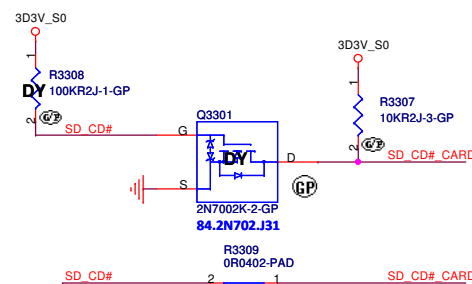
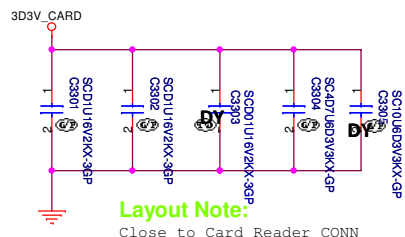
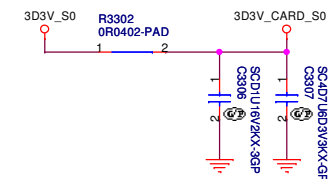
Date: Monday, November 09, 2015 Sheet 32 of 109

SSID = Card Reader

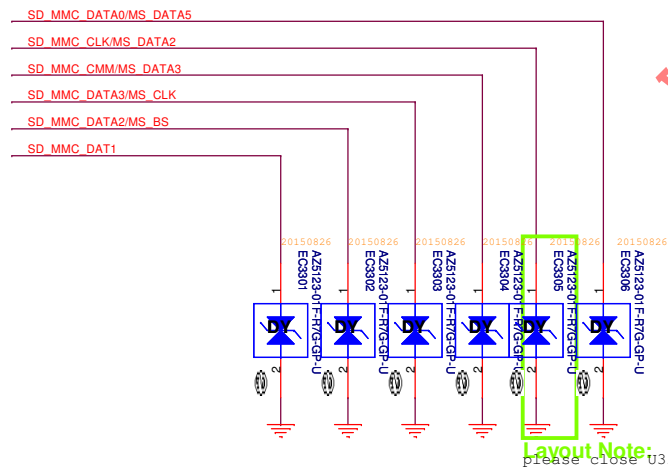


SD Card Connector

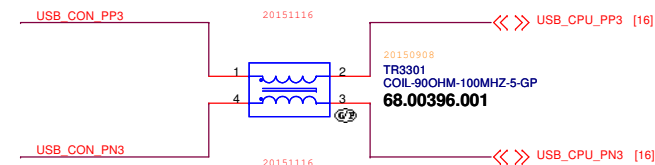
Pin Define	
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



For EMI Reserved



Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



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Title	Card Reader + CONN
-------	---------------------------

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SSID = USB

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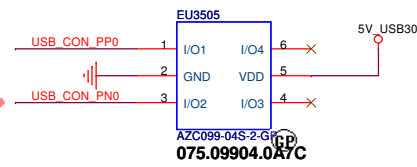
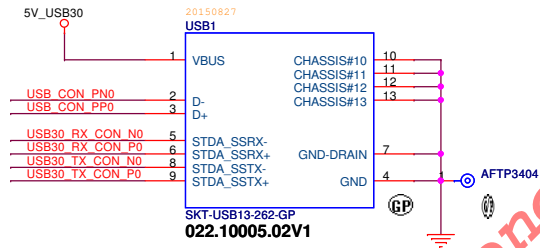
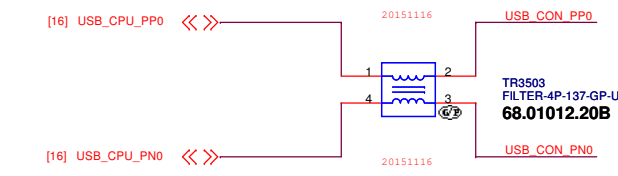
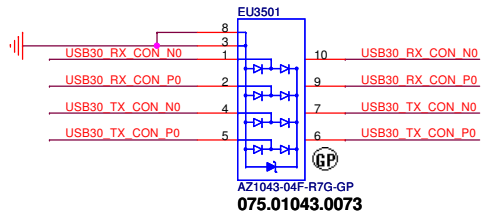
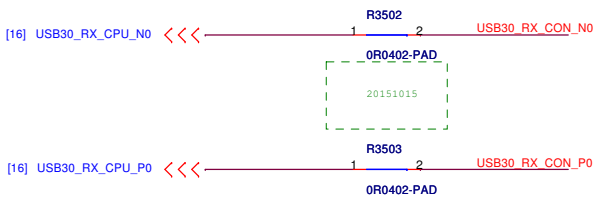
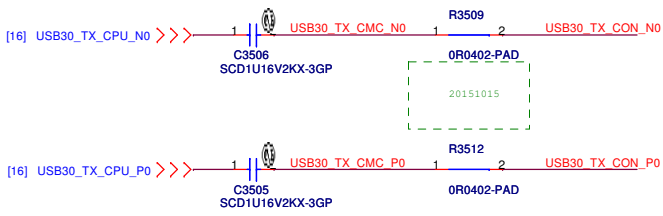
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Title
(Reserved)USB 2.0 Port

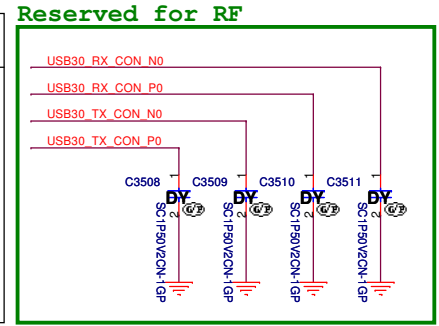
Size A4	Document Number Rocket BSW 11.6"	Rev A00
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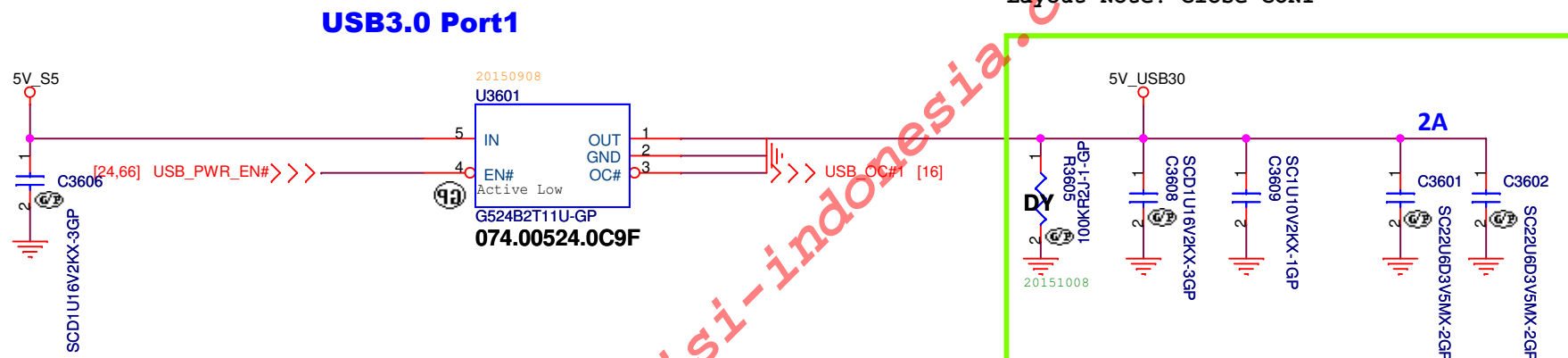
SSID = USB



USB 3.0 Connector	
Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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Title

USB Power SW

Size
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SSID = USB

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Title			
USB2.0 HUB			
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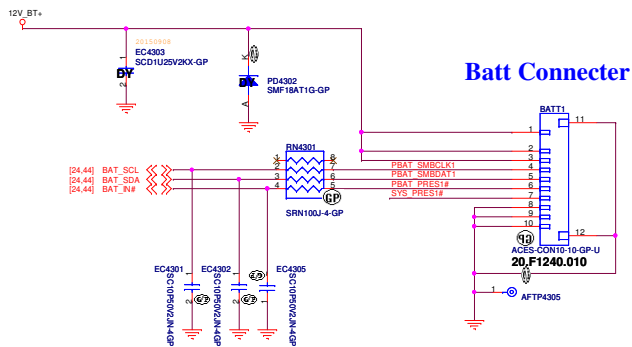
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Title **(Reserved)**

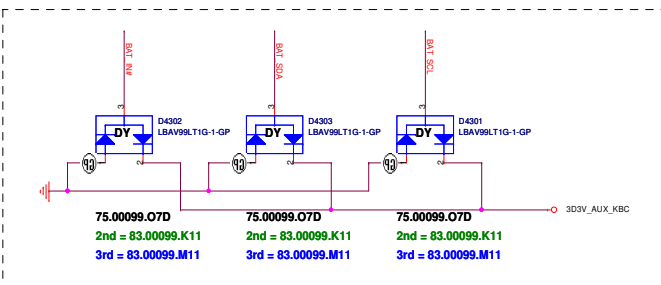
Size A4	Document Number Rocket BSW 11.6"	Rev A00
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```
SSID = PWR.Support
```



Placement: Close to Batt Connector



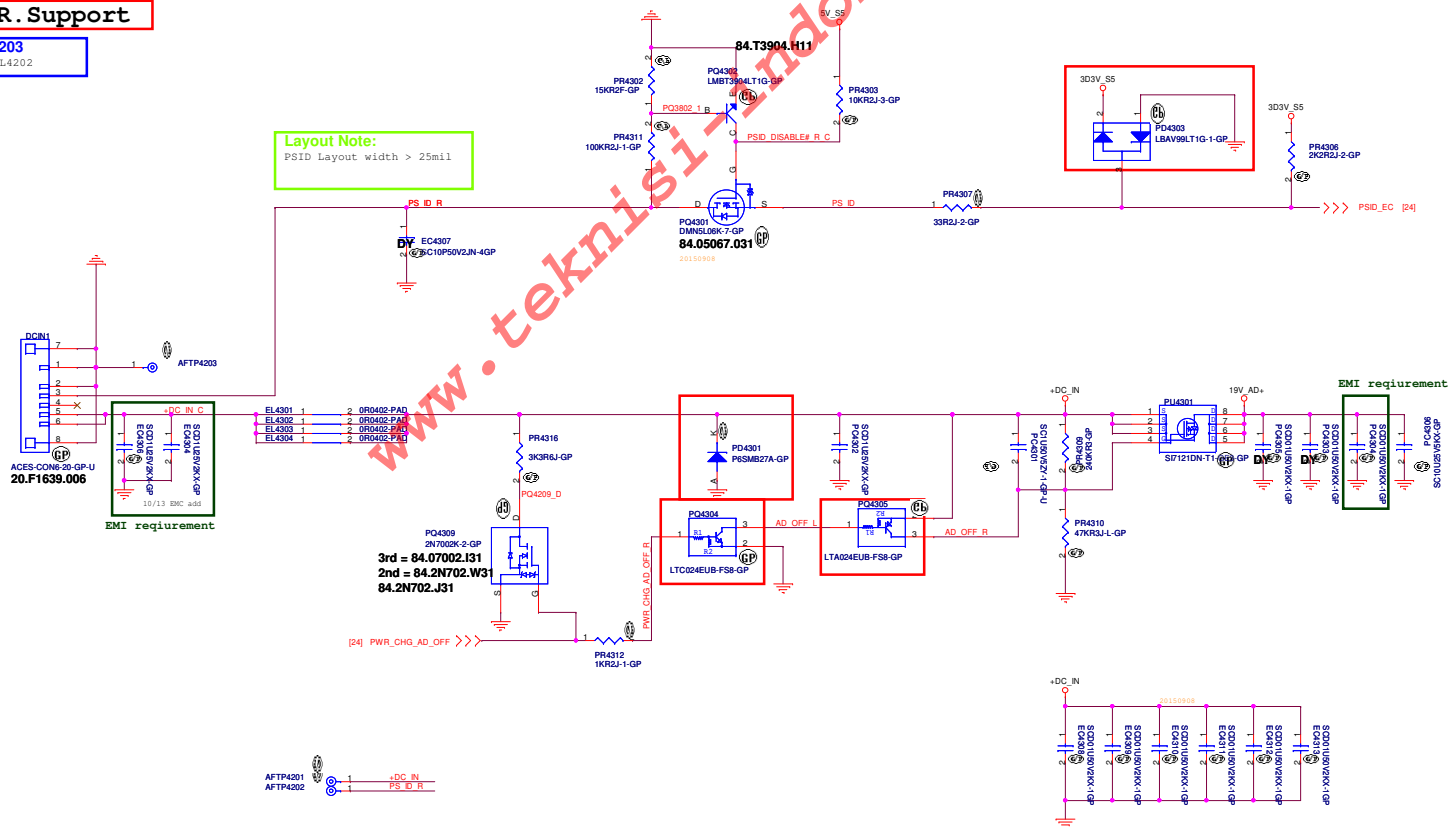
SSID = PWR.Support

0103 Add EC4203

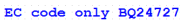
ndde close to EL420

Layout Note:

PSID Layout width > 25mil

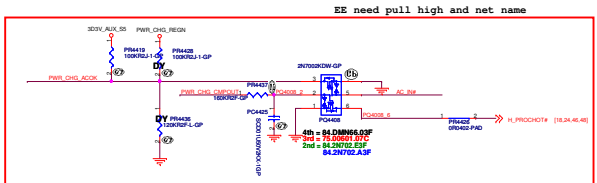


Main Func = Charger



H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1

Charger Current=1.4~3.6A

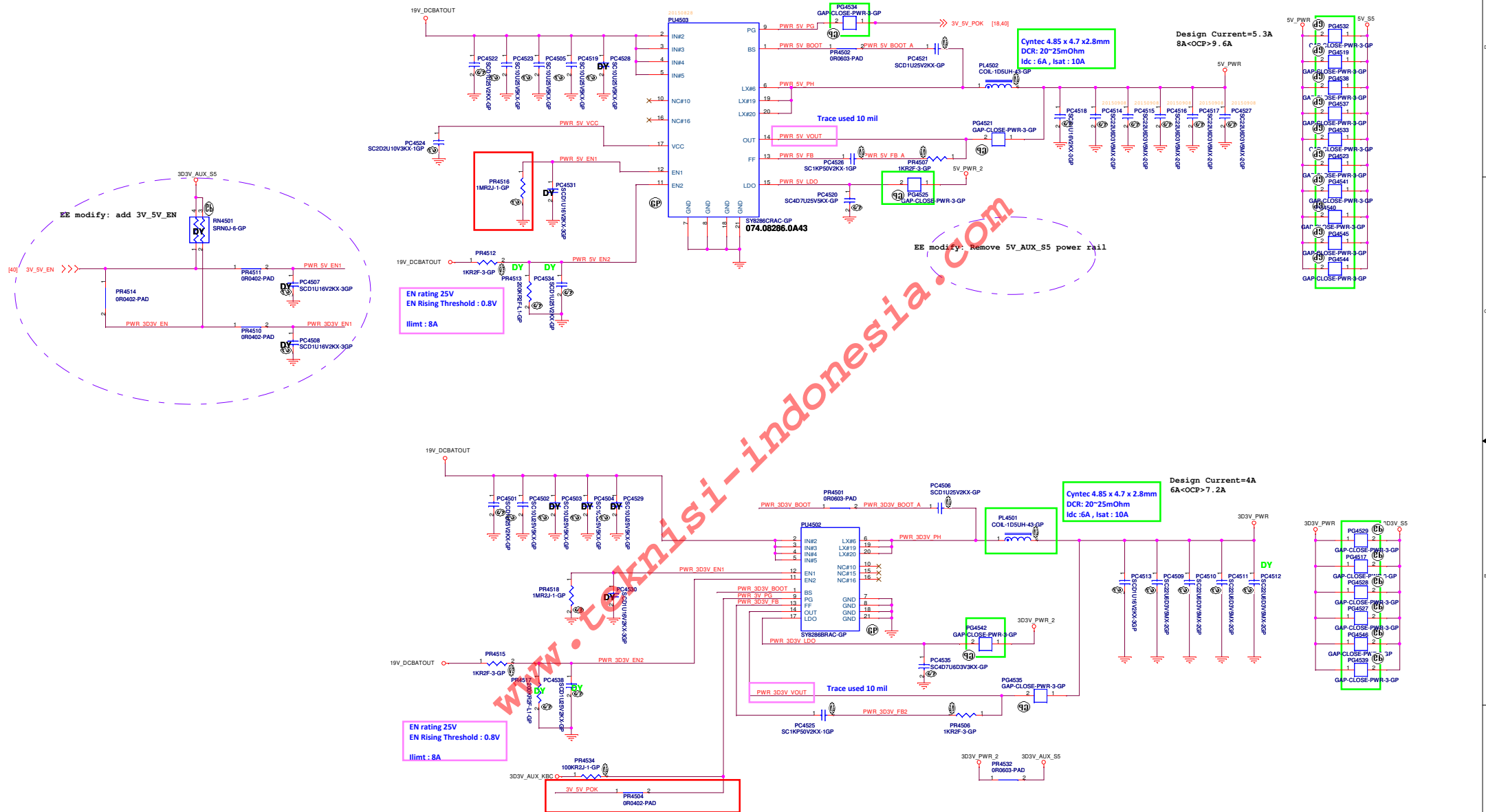


EE need pull high and net name

Customer Request

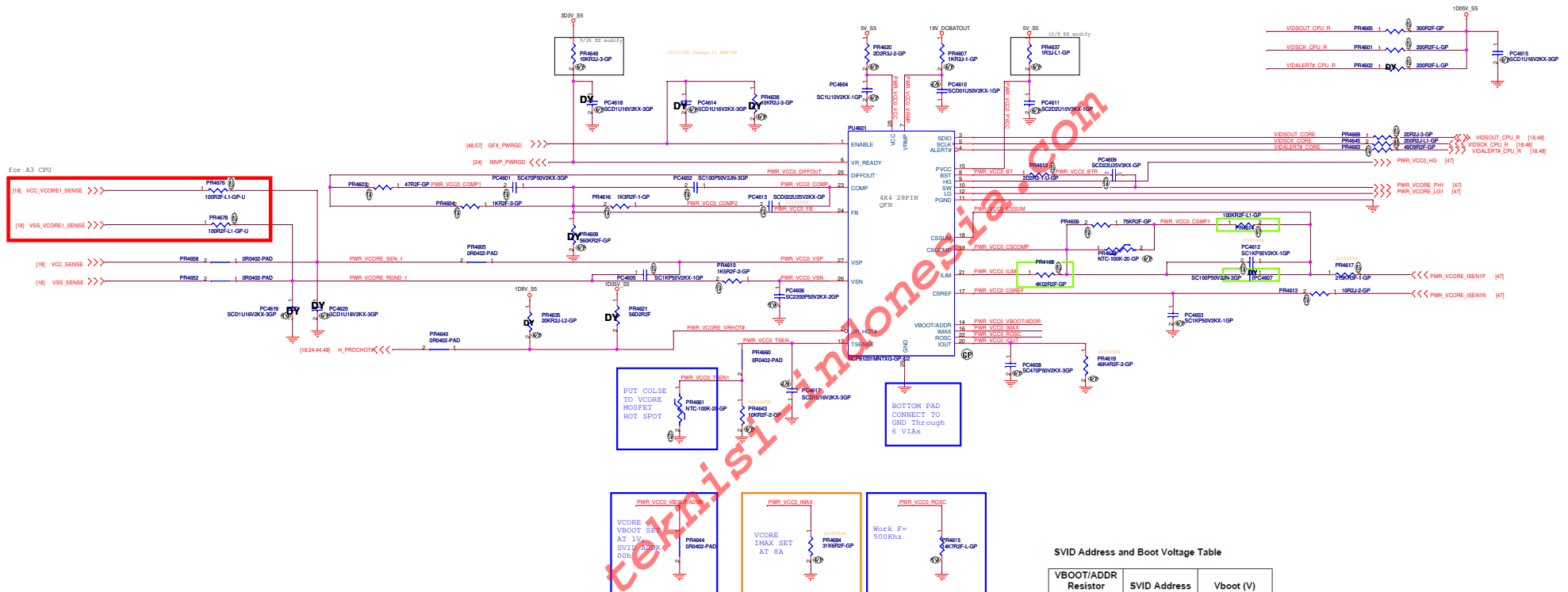
Close PR4416

BATTERY MON



<Core Design>

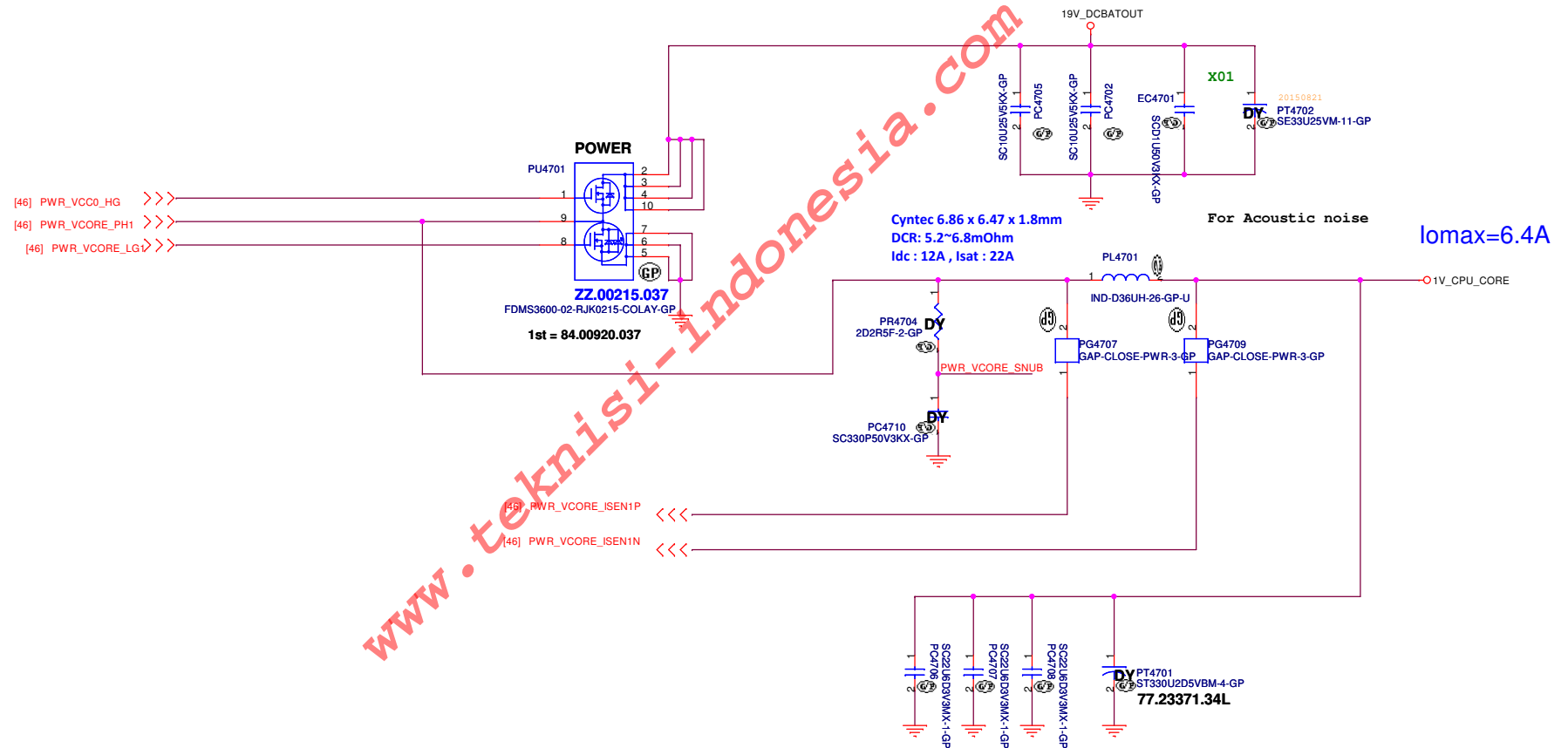
SSID = CPU Regulator



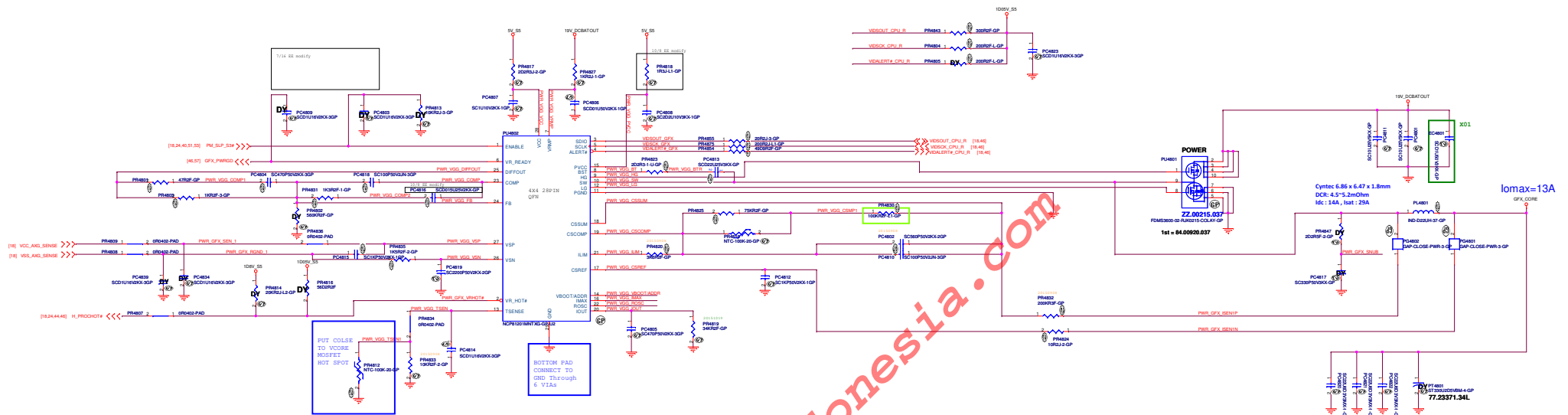
SVID Address and Boot Voltage Table

VBOOT/ADDR	SVID Address	Vboot (V)
Resistor (Ohm)		
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.8 k	0x6	1.0
68.1 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x0	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
178 k	0x7	1.1
198 k	0x8	1.1

SSID = CPU Regulator



SSID = GFX Regulator



SVID Address and Boot Voltage Table

VBOOT/ADDR	Vboot Pin Voltage (mV)				SVID Address	Vboot (V)
Resistor (Ohms)	Min	Typ	Max			
0	0	0	102	0x0	1.0	1.0
14.0 k	102	140	102	0x1	1.0	1.0
22.1 k	180	219	258	0x2	1.0	1.0
30.1 k	258	304	343	0x3	1.0	1.0
39.2 k	344	391	431	0x4	1.0	1.0
48.7 k	438	484	531	0x5	1.0	1.0
57.8 k	531	578	625	0x6	1.0	1.0
68.1 k	625	676	727	0x7	1.0	1.0
78.7 k	727	781	838	0x8	1.0	1.0
88.7 k	838	894	953	0x9	1.0	1.0
100 k	953	1022	1092	0xA	1.1	1.1
113 k	1062	1125	1188	0xB	1.1	1.1
128 k	1188	1260	1332	0xC	1.1	1.1
137 k	1312	1378	1445	0xD	1.1	1.1
150 k	1445	1511	1578	0xE	1.1	1.1
165 k	1578	1648	1719	0xF	1.1	1.1
178 k	1719	1789	1859	0x7	1.1	1.1
196 k	1859	1950		0x8	1.1	1.1

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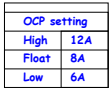
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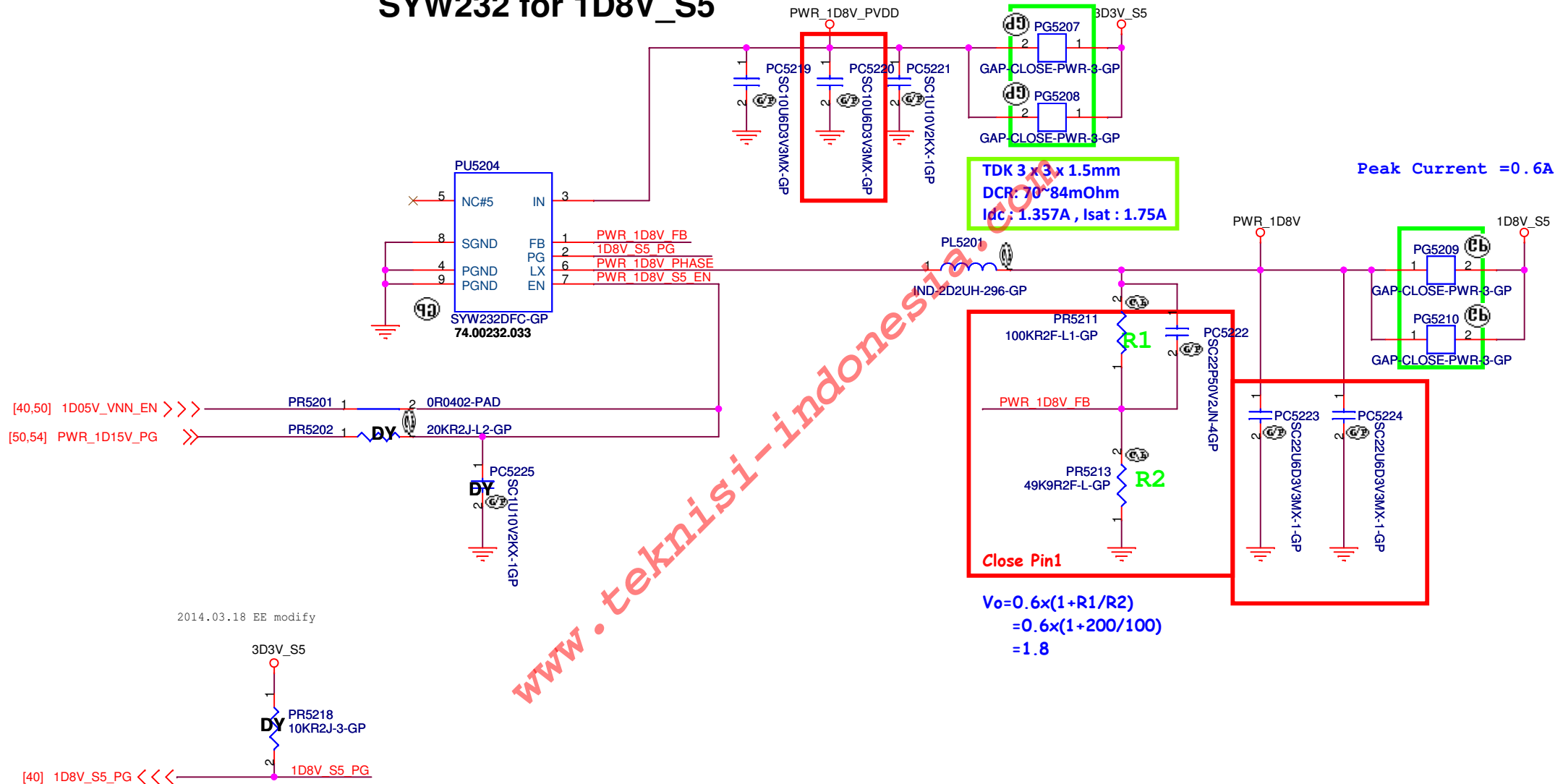
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Title			(Reserved)		
Size	Document Number				Rev
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[illegible]

SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D8V_S5



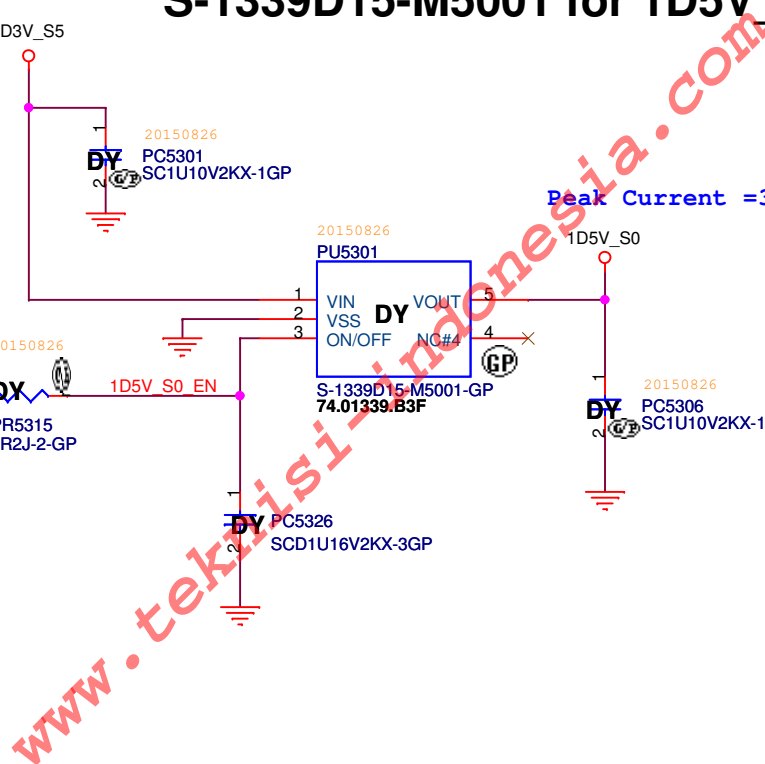
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Title			
SYW232DFC_1D8V			
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Size A4	Document Number <div style="text-align: center;"> <i>Rocket BSW 11.6"</i> </div>	Rev <div style="text-align: center;"> <i>A00</i> </div>	
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Title

S1339D15 1D5V

Size
A4

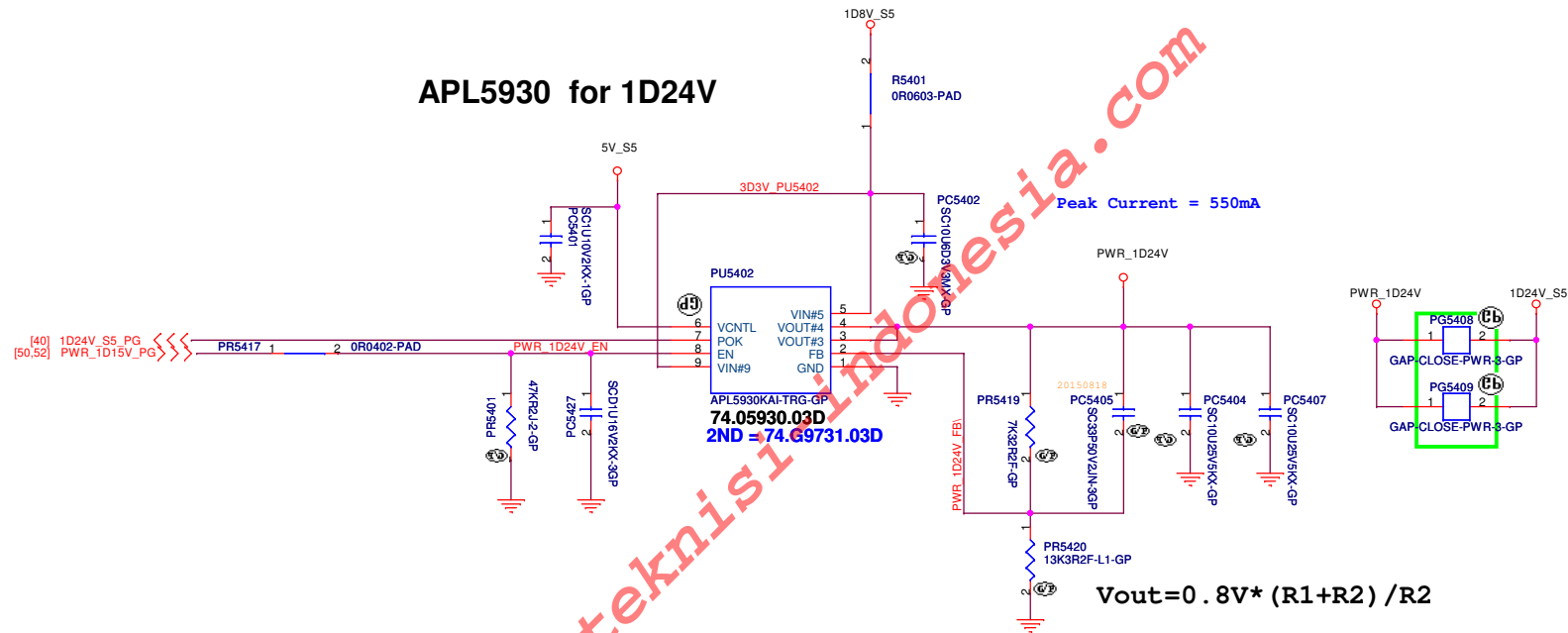
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APL5930 for 1D24V



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Document Number

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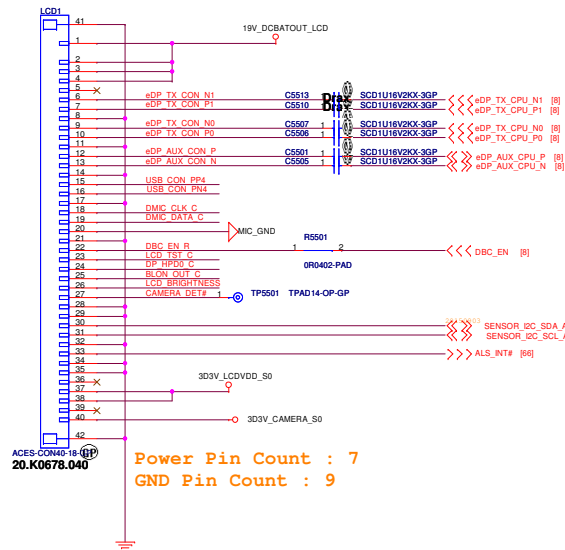
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Date: Monday, November 09, 2015

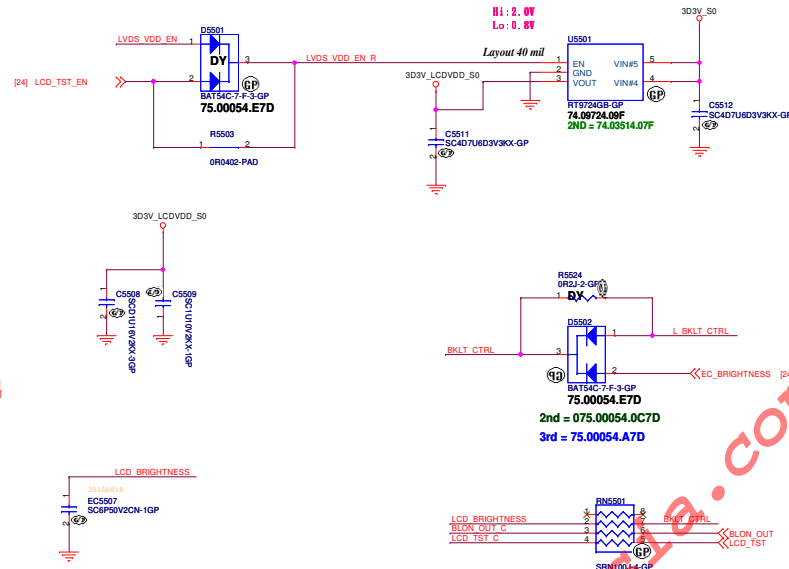
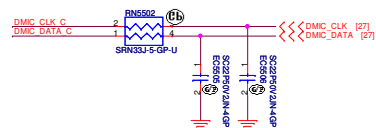
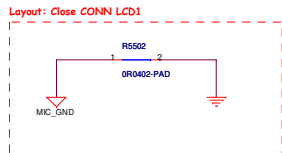
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SSID = VIDEO

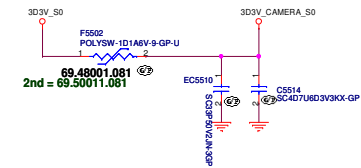
Panel Conn.



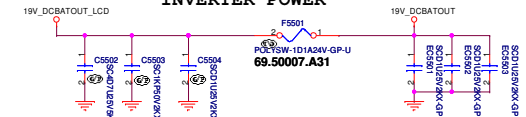
```
Power Pin Count : 7
GND Pin Count : 9
```



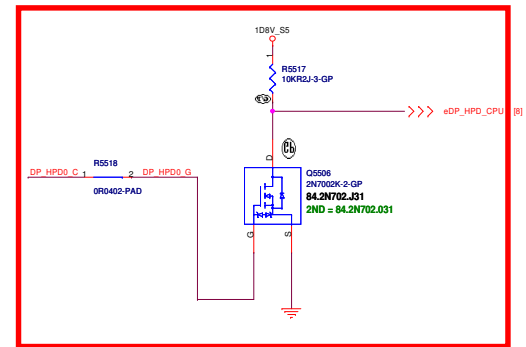
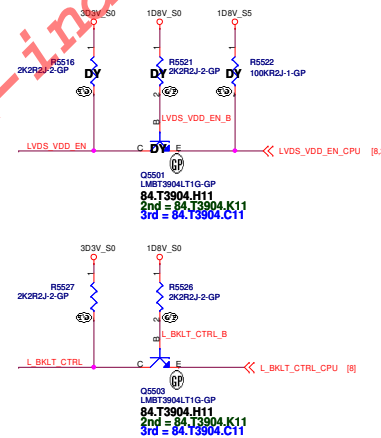
CAMERA POWER



INVERTER POWER



Level shift



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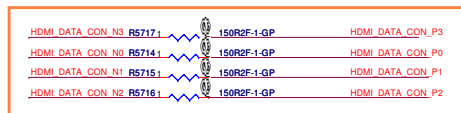
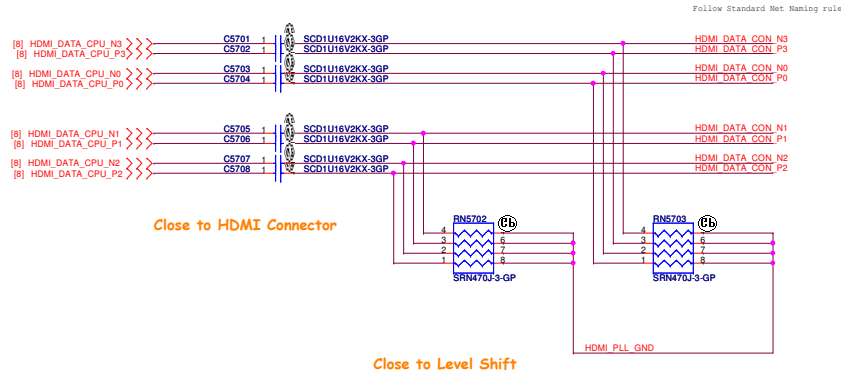
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Rev
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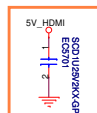
Date: Monday, November 09, 2015

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HDMI Level Shifter & CONNECTOR

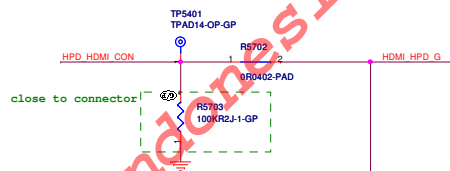
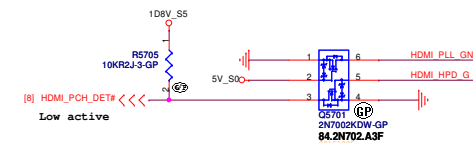
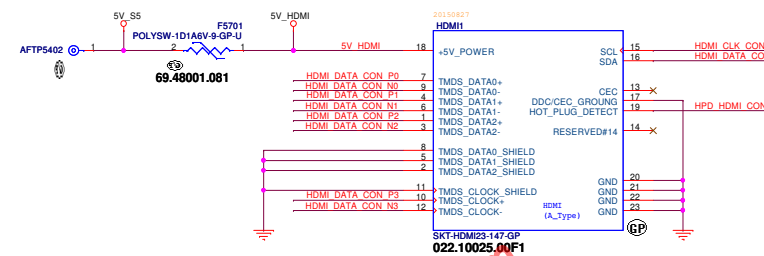


Reserve 150 ohm bridge resistance
on the HDMI trace as circle for EMI

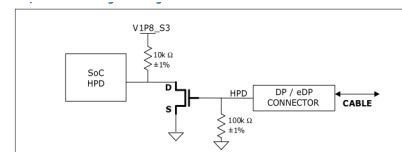
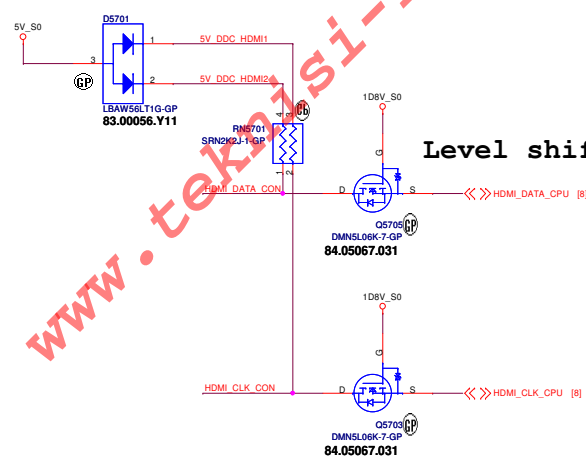


Reserve 0.1uF for ESD

HDMI CONN



Level shift



NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage $\leq 1.5V$.

NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms $\pm 20\%$

Table 4-39 Required Detection Levels for Hot Plug Detect Signal


Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts

SSID = Display Port

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Title (Reserved) Display Port			
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SSID = DVI

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Title **(Reserved) DVI**

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SSID = SATA

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Title

HDD

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SSID = WWAN

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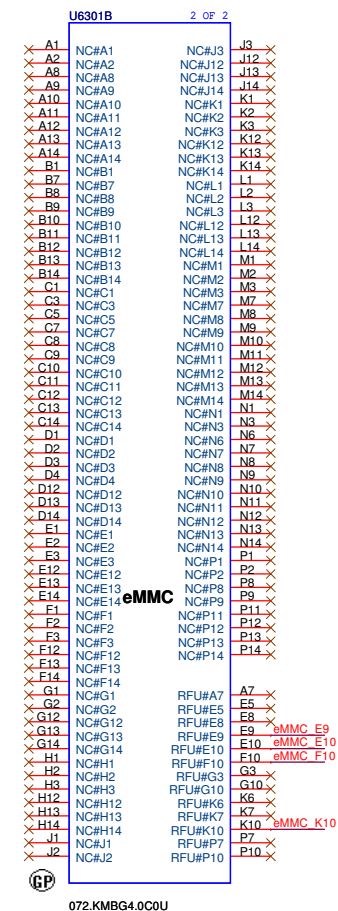
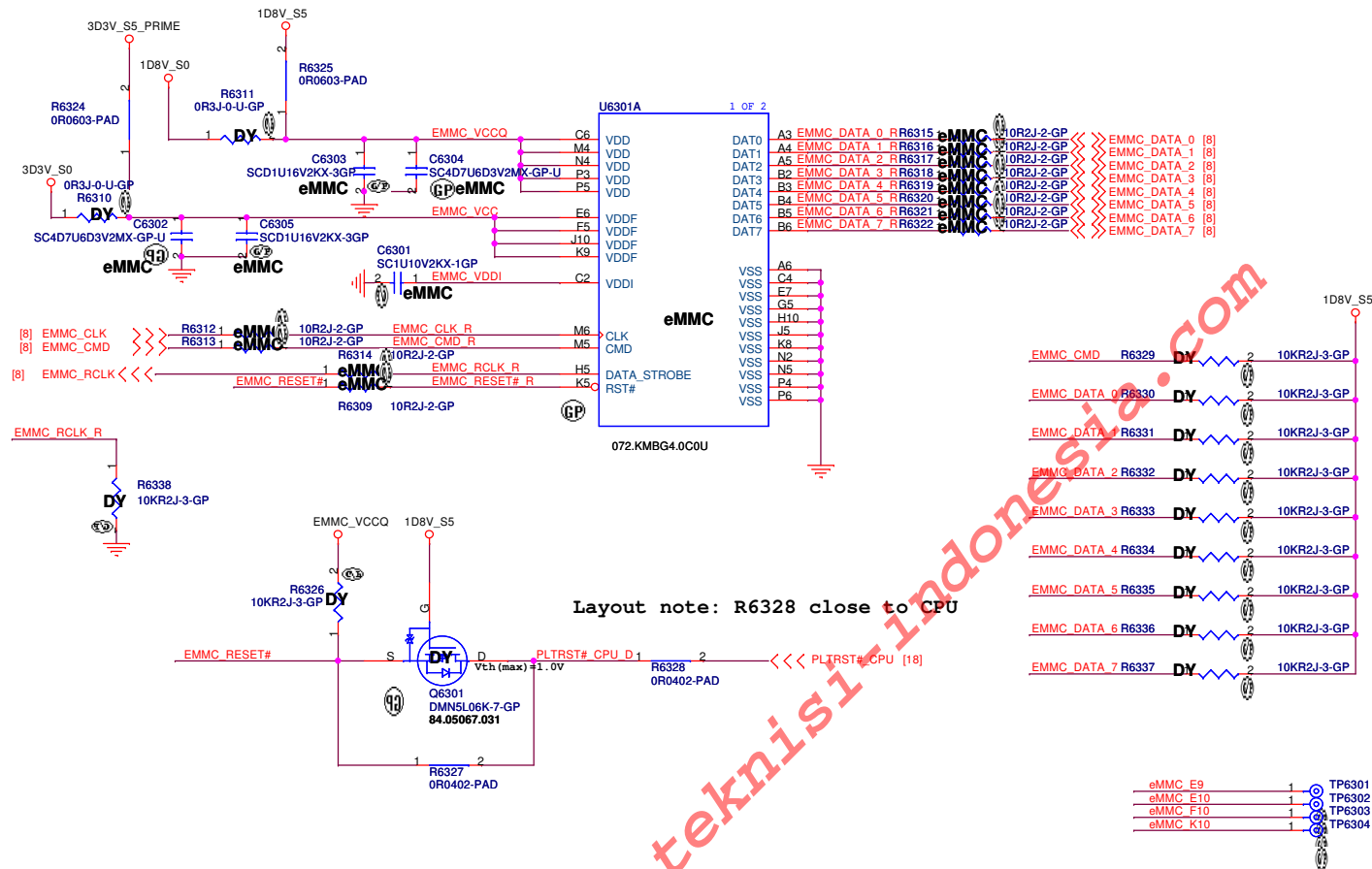
Rev

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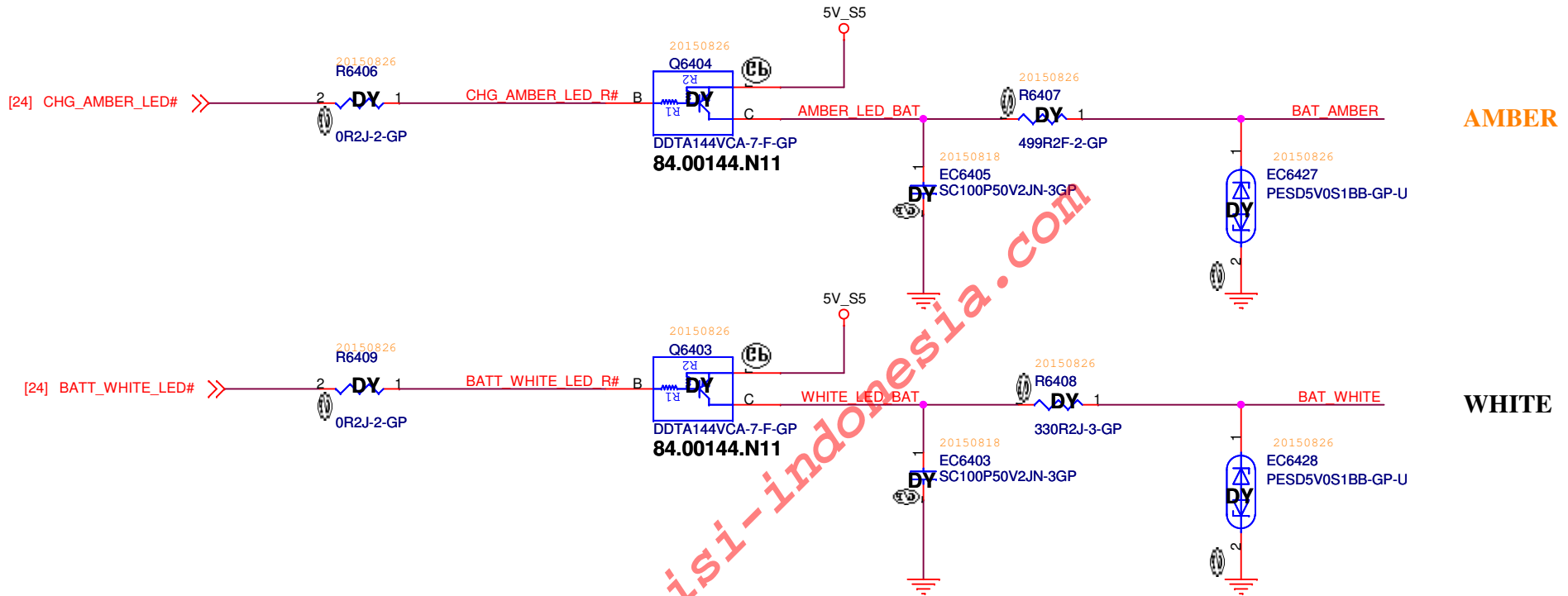
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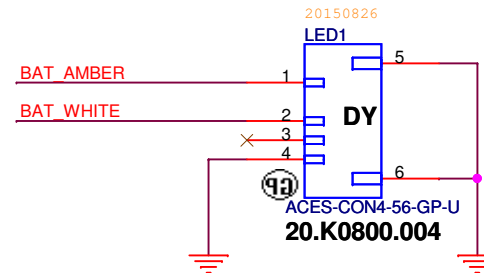
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CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V		BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V		BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4T		BRASWELL 4c FCBGA 1.6GHz 6W, GT 16EU, PENTIUM QS QJ4S	
eMMC	Hynix/32G		Hynix/32G		SanDisk/32G		Samsung/32G	
	J6PD1		J6PD1		4P0NC		N8DV6	
	SKU7		SKU8		SKU9			
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V		BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V		BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4T			
eMMC	Hynix/64G		SanDisk/64G		Samsung/64G			
	WF56J		7F7DJ		67D71			

SSID = LED / PWRBTN

Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO



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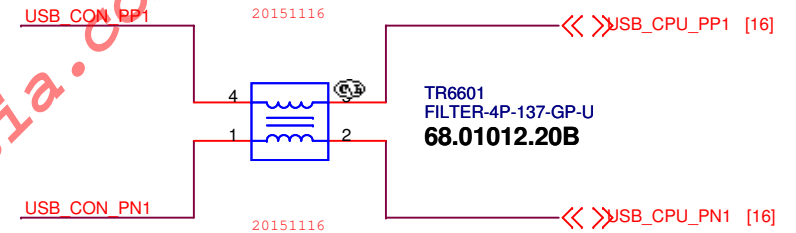
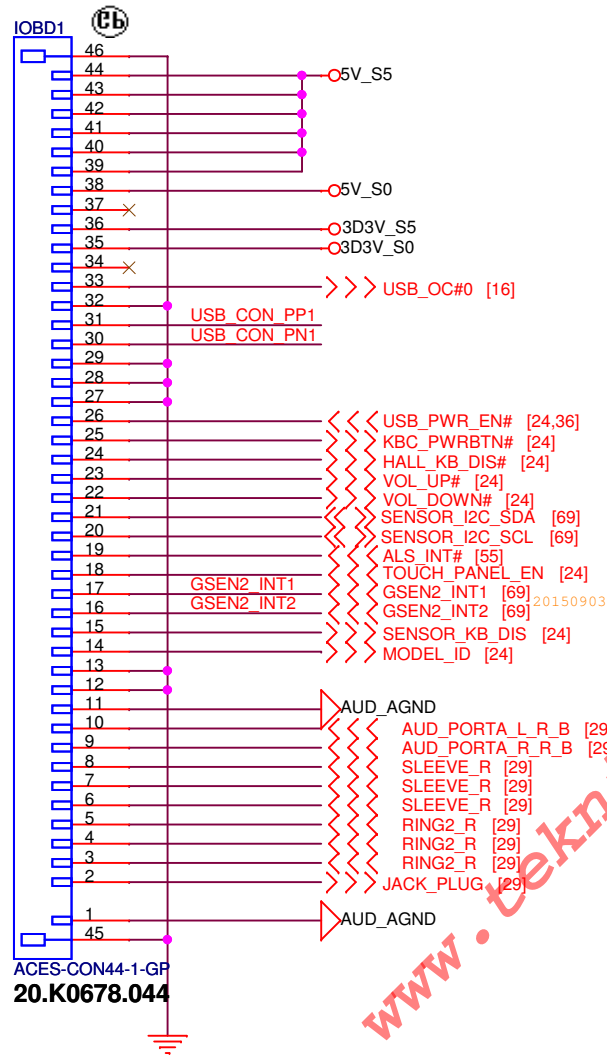


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Title
LED / PWRBTN

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Power Pin Count : 10
GND Pin Count : 5

USB3.0 Port2

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Title

IO Board CONN

Size
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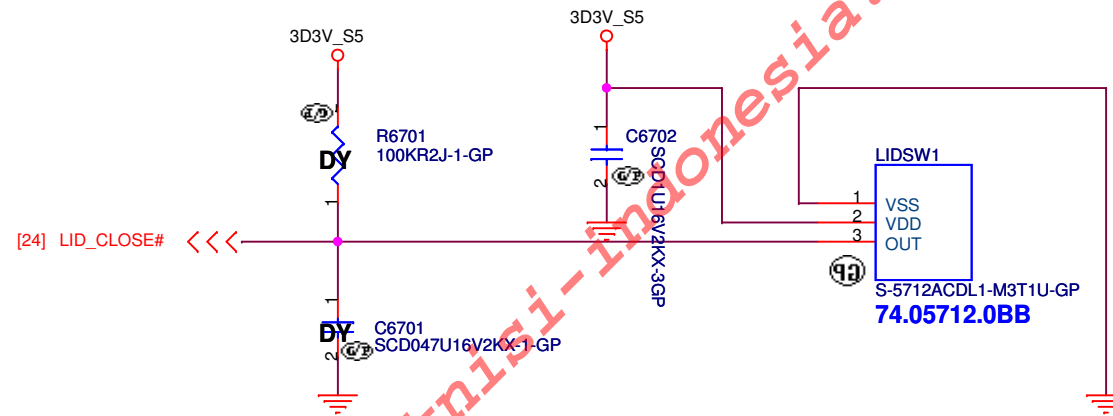
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Title

Hall Sensor

Size
A4

Document Number

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SSID = Debug CONN

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Title

(Reserved) Debug CONN

Size
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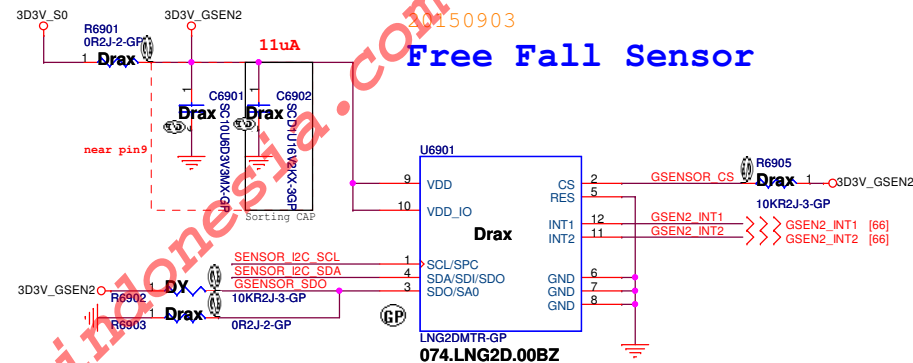
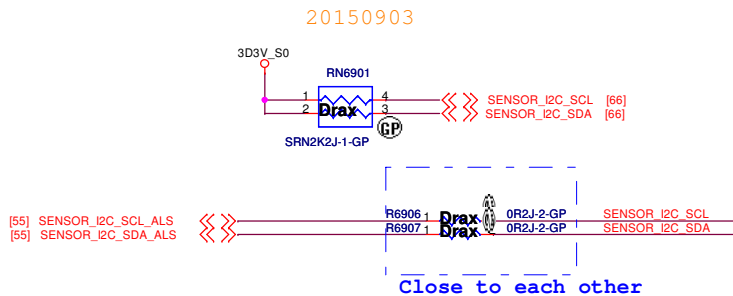
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SSID = Sensor




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SSID = Free Fall Sensor

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Title			
Free Fall Sensor			
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Title (Reserved)Thunderbolt (1/5)			
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Title (Reserved)Thunderbolt (2/5)			
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Title (Reserved)Thunderbolt (3/5)			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
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Title (Reserved)Thunderbolt (4/5)		
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Title **(Reserved)Thunderbolt (5/5)**


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Title (Reserved)GPU (1/5) PEG			
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Title (Reserved)GPU (2/5) DIGITAL		
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Title **(Reserved)GPU (3/5) VRAM**


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Title (Reserved)GPU (4/5) GPIO			
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Title **(Reserved)GPU (5/5) PWR/GND**


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Title **(Reserved)VRAM5,6 (3/4)**

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Title **(Reserved)VRAM7,8 (4/4)**


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Title (Reserved)DISCRETE VGAPOWER			
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SPRING-171-GP
SPR1



20150827

34.4YW18.001

SPRING-171-GP
SPR2



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34.4YW18.001

SPRING-171-GP
SPR3



20151008

34.34S02.002

SPRING-98-GP
SPR4



20151008

34.34S02.002

SPRING-98-GP
SPR5



20151008

34.34S02.002

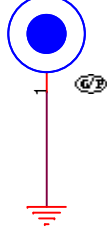
SPRING-98-GP
SPR6



20150901

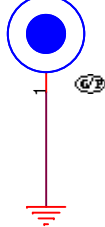
ZZ.PAD01.041

H1
HOLE354R237-GP



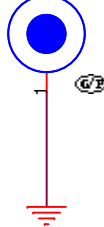
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H2
HOLE256R142-OG-1-GP



ZZ.00PAD.7L1

H4
HOLE335R197-GP



ZZ.00PAD.7L1

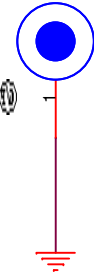
H9
HOLE335R197-GP



20151012 Remove H12 H14

34.4OX45.101

HS1
STF237R117H67-3-GP



34.4OX45.101

HS2
STF237R117H67-3-GP



34.4OX45.101

HS3
STF237R117H67-3-GP



34.4OX45.101

HS4
STF237R117H67-3-GP



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Title

UNUSED PARTS/EMI Capacitors

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Title **(Reserved)NFC Connector**

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Title **(Reserved)Finger Print**

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(Reserved)Express Card

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Title		
(Reserved)Smart Card Socket		
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Title (Reserved)SW GFX eDP		
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Title ***(Reserved)Bottom Docking***


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Title (Reserved)LAN			
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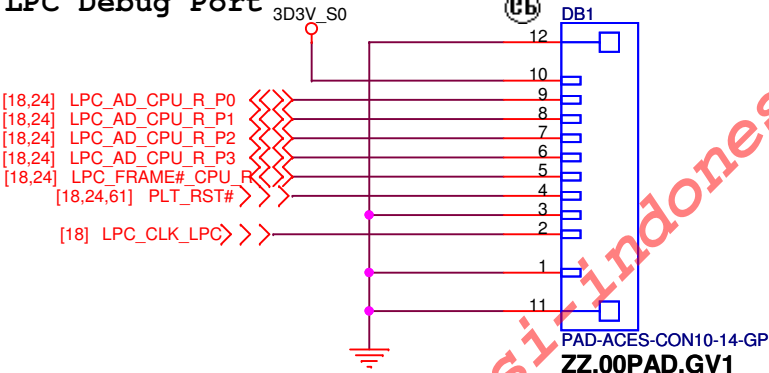
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Title (Reserved)LAN SWITCH					
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SSID = DEBUG PORT

LPC Debug Port



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

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Title

CPU_XDP

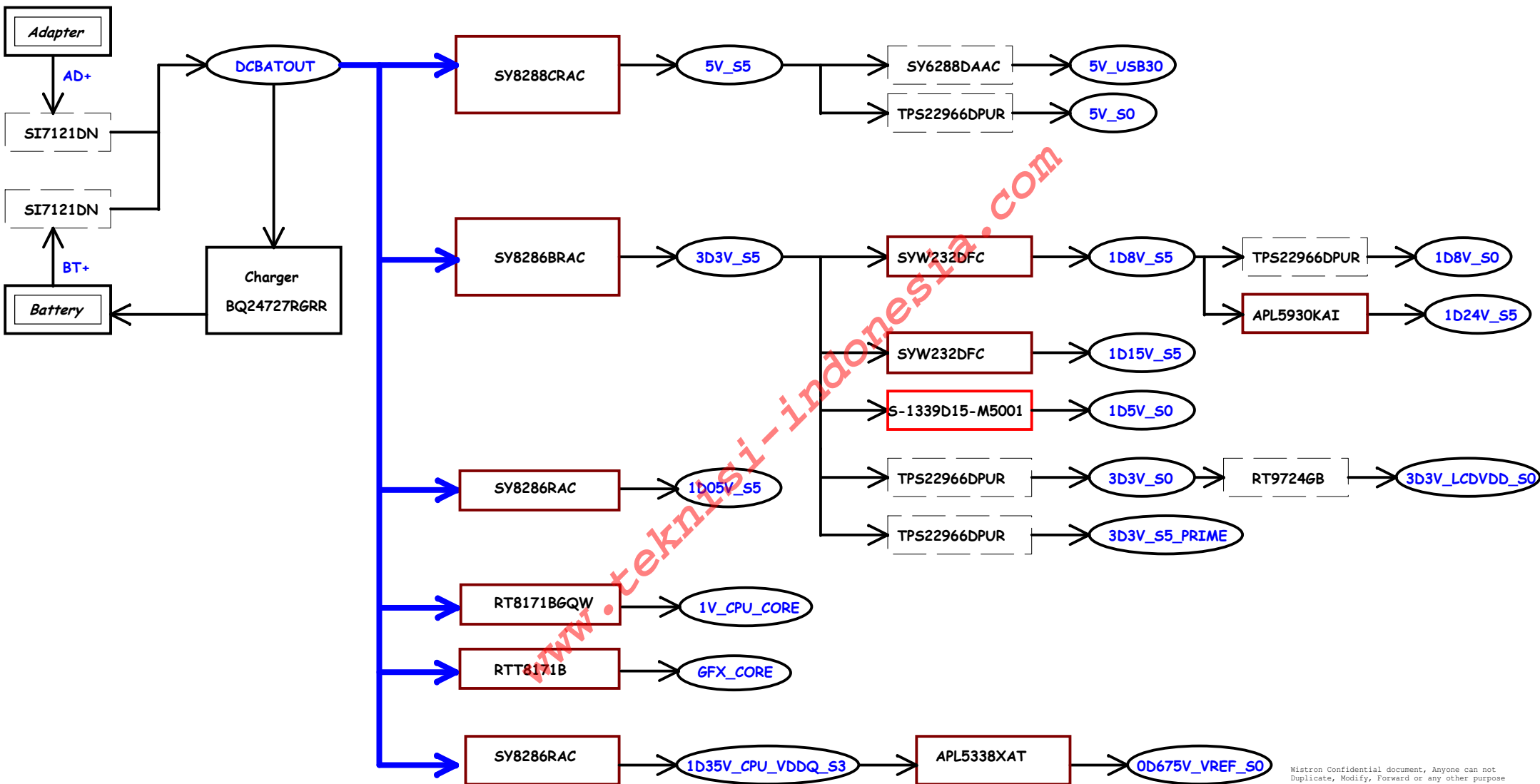
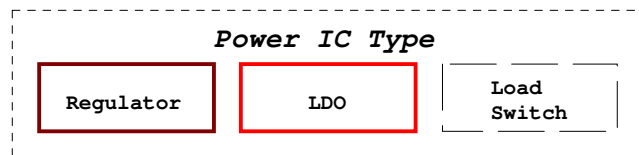
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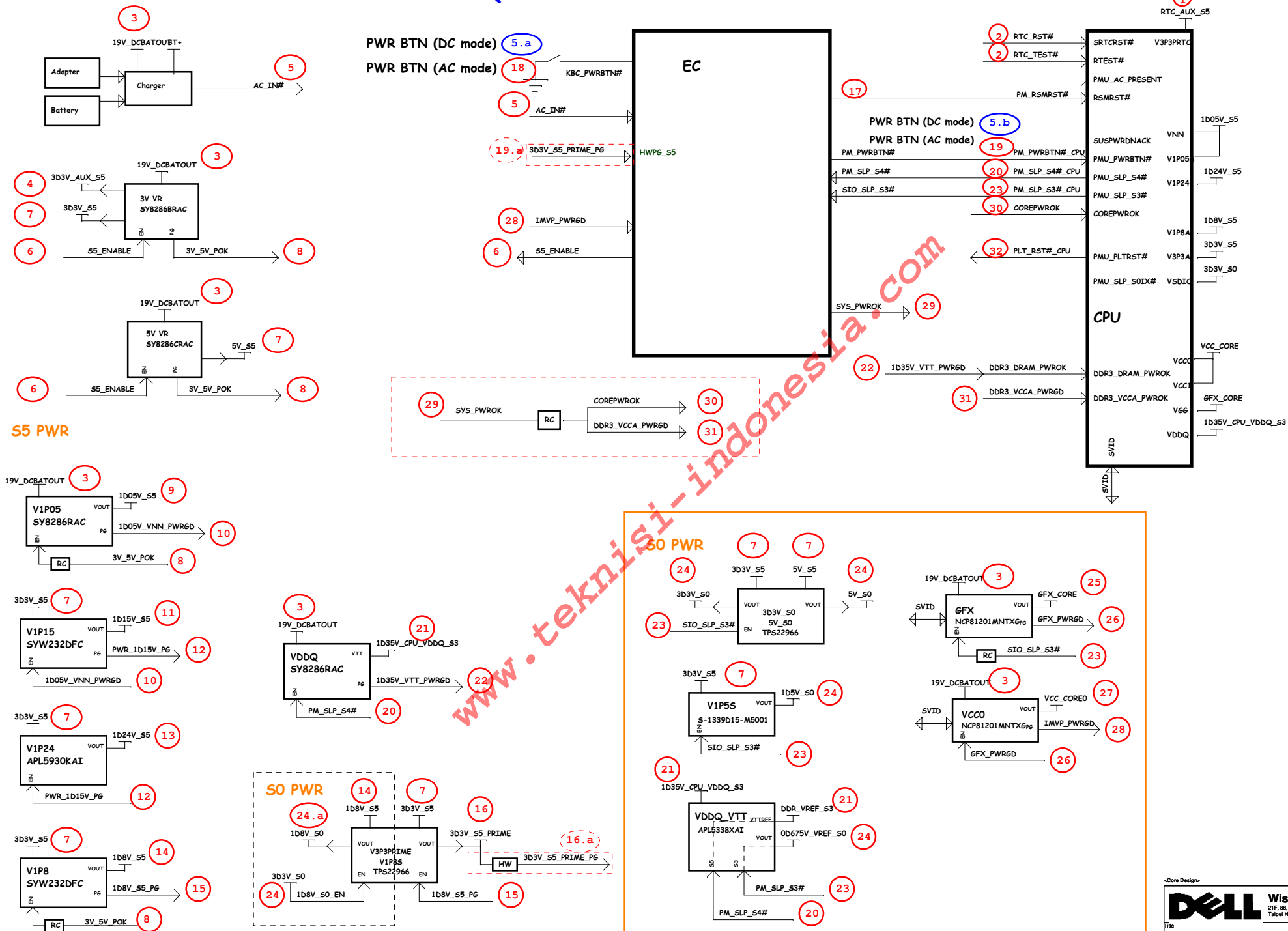
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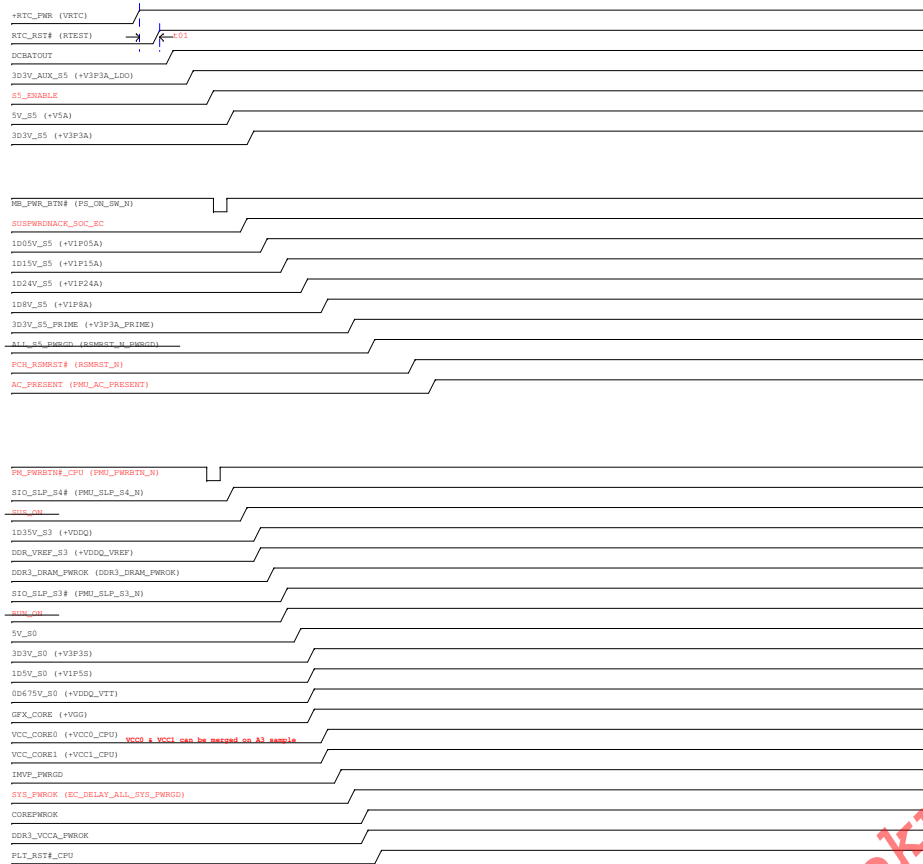


Title			Power Block Diagram	
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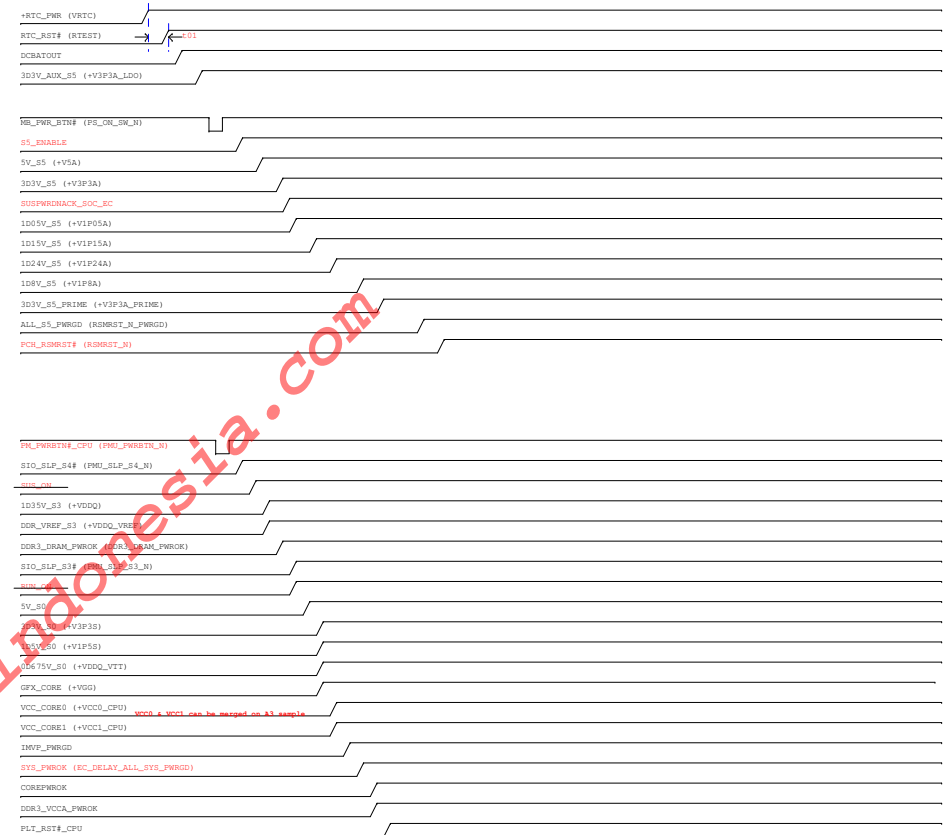
Braswell POWER UP SEQUENCE DIAGRAM



(AC mode) Red word : KBC GPIO



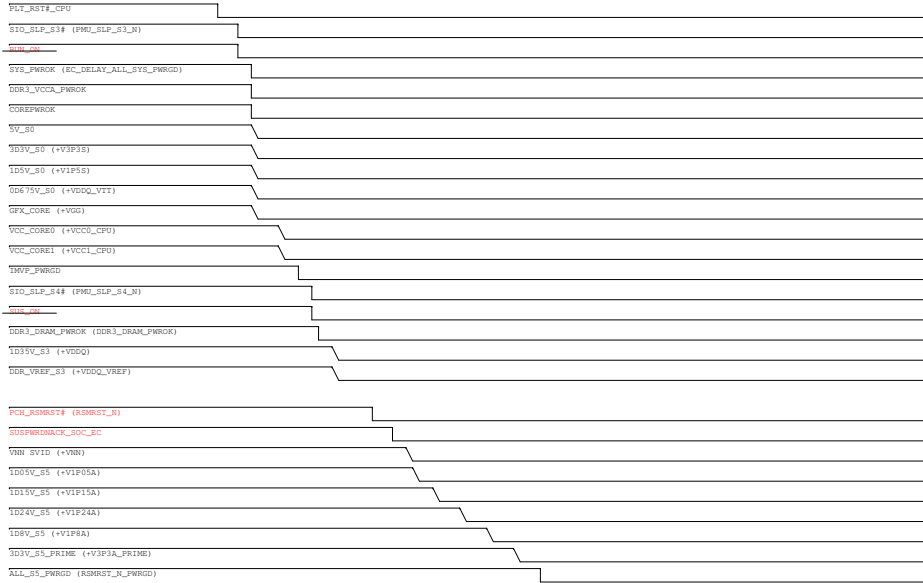
(DC mode) Red word : KBC GPIO



Intel-Power Down Sequence

(AC mode)

Red word : XBC QP10



Intel-Power Down Sequence

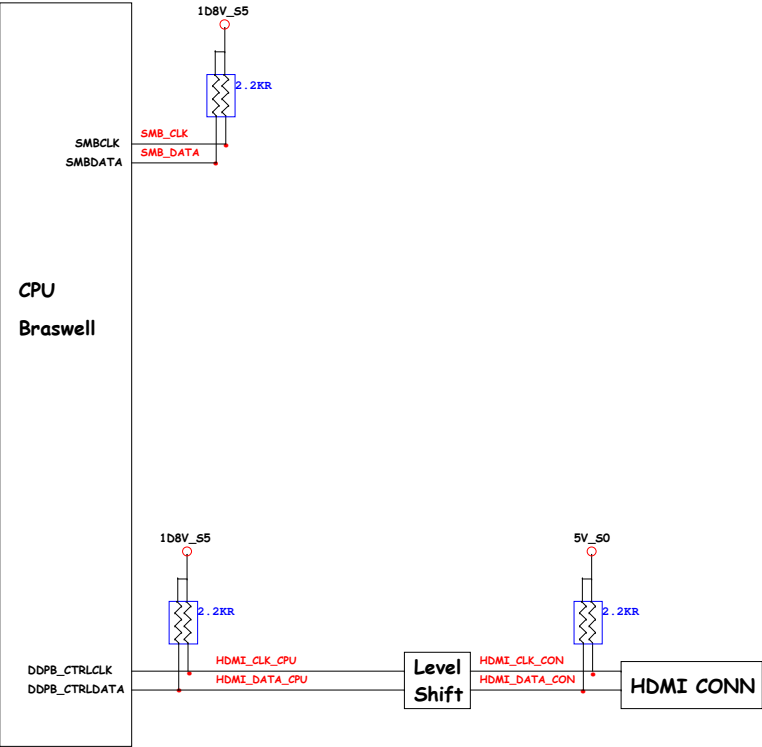
(DC mode)

Red word : XBC QP10

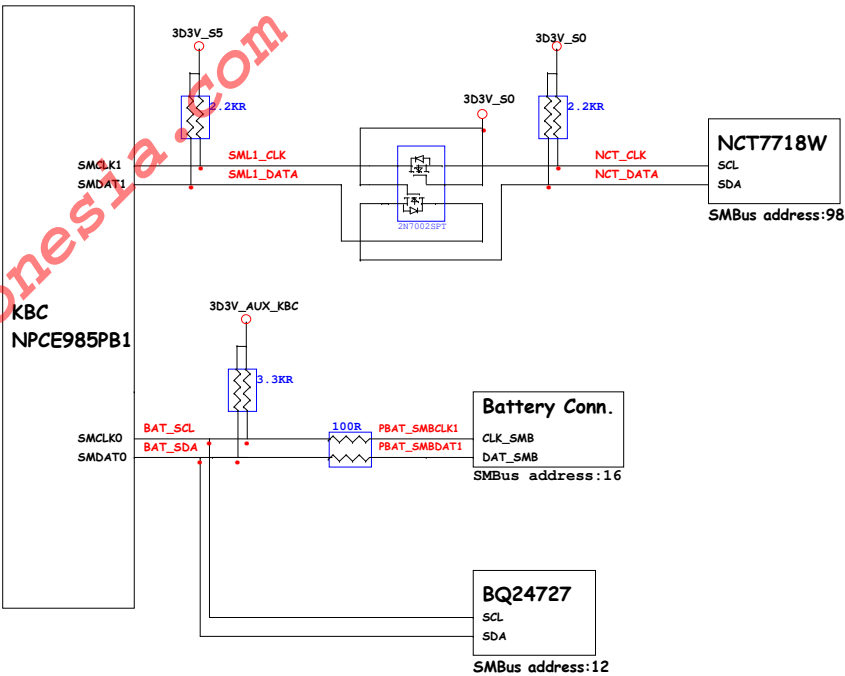


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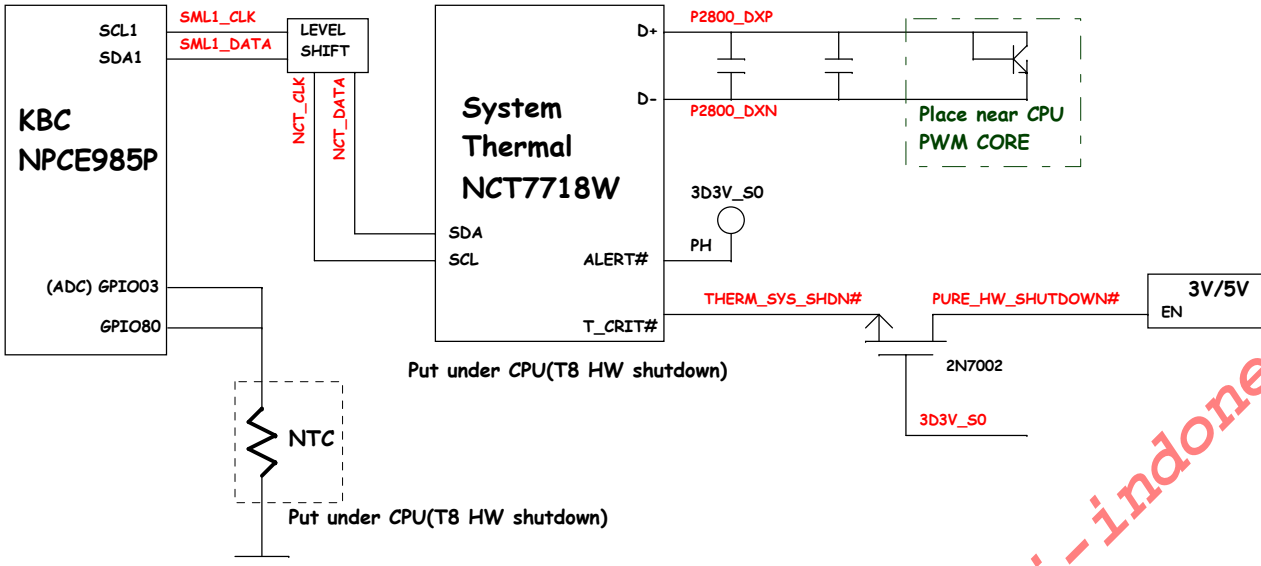
PCH SMBus Block Diagram



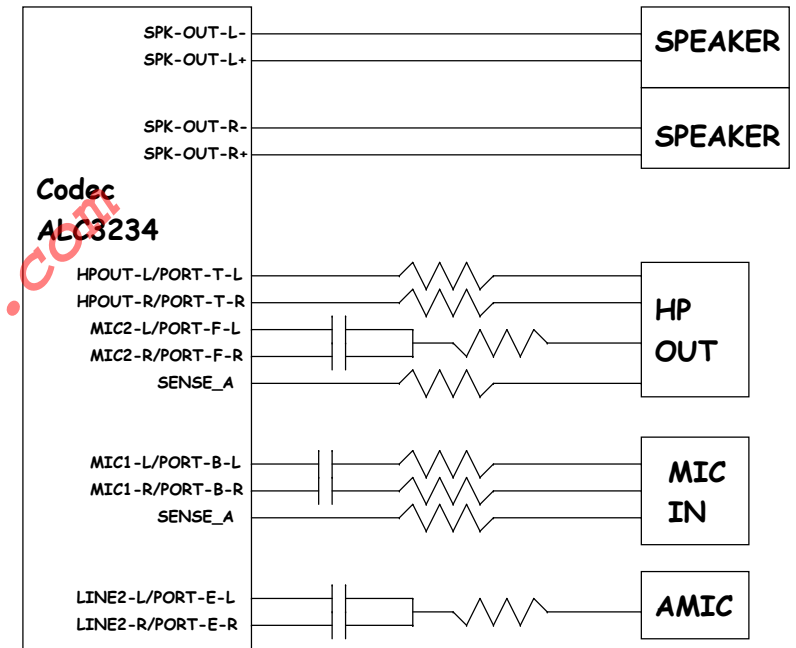
KBC SMBus Block Diagram



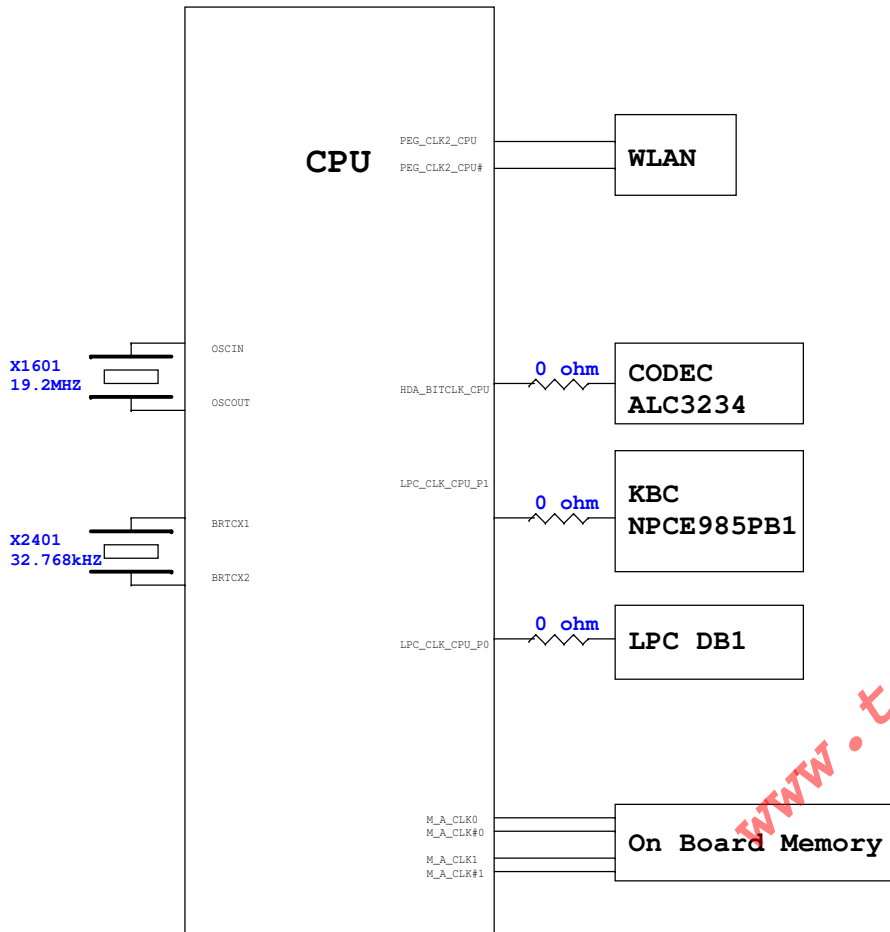
Thermal Block Diagram



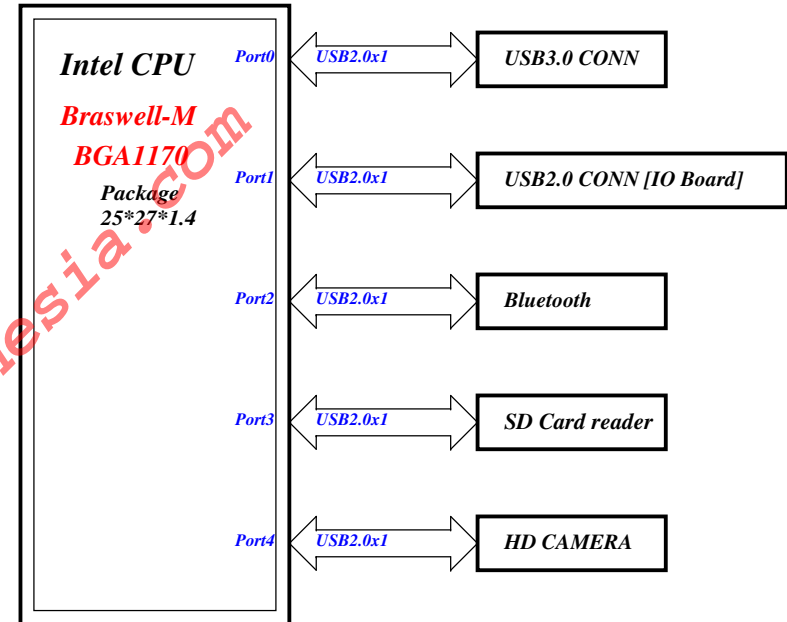
Audio Block Diagram



CLK Block Diagram



USB2.0 Port Block Diagram



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CLK / SENSOR Block

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